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MS-7A64

ATX

Ver: 10

Intel -Kabylake plamform B250/H270

CPU:

kabylake-S

System Chipset:

B250/H270

Onboard Chip:

HD Audio Codec:ALC1220
LAN:INTEL I219
SIO:Nuvoton 6795
Flash ROM: SPI 128MB

Main Memory:

*DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)*

ACPI:

NIKO/UPI

PWM:

UPI9508

Expansion Slots:

*PCI Express (X16) Slot *1*
*PCI Express (X4) Slot *1*
*PCI Express (X1) Slot * 2*
*PCI Slot * 2*
*M2 * 2*

Other:

SATA3.0 x6 (PCH)
*FRONT USB2.0 *4*
*FRONTUSB3.0 *4*
*REAR USB3.0 (B250*2/H270*4)*
*REAR USB2.0 *2*
REAR USB TYPE A+C

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size: Custom | Document Description: Cover Sheet | Rev: 10

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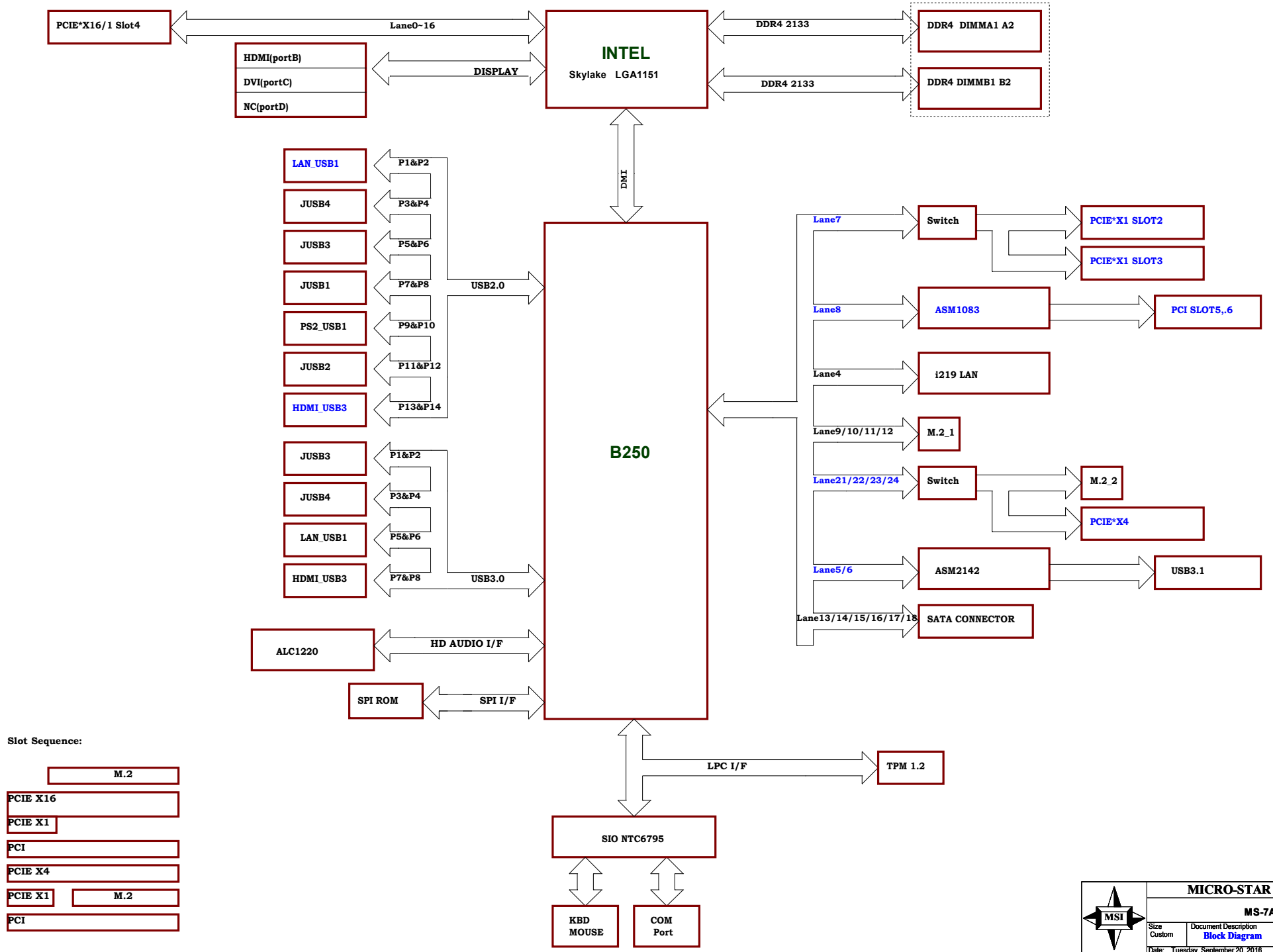
MS-7A64 Block Diagram



Slot Sequence:

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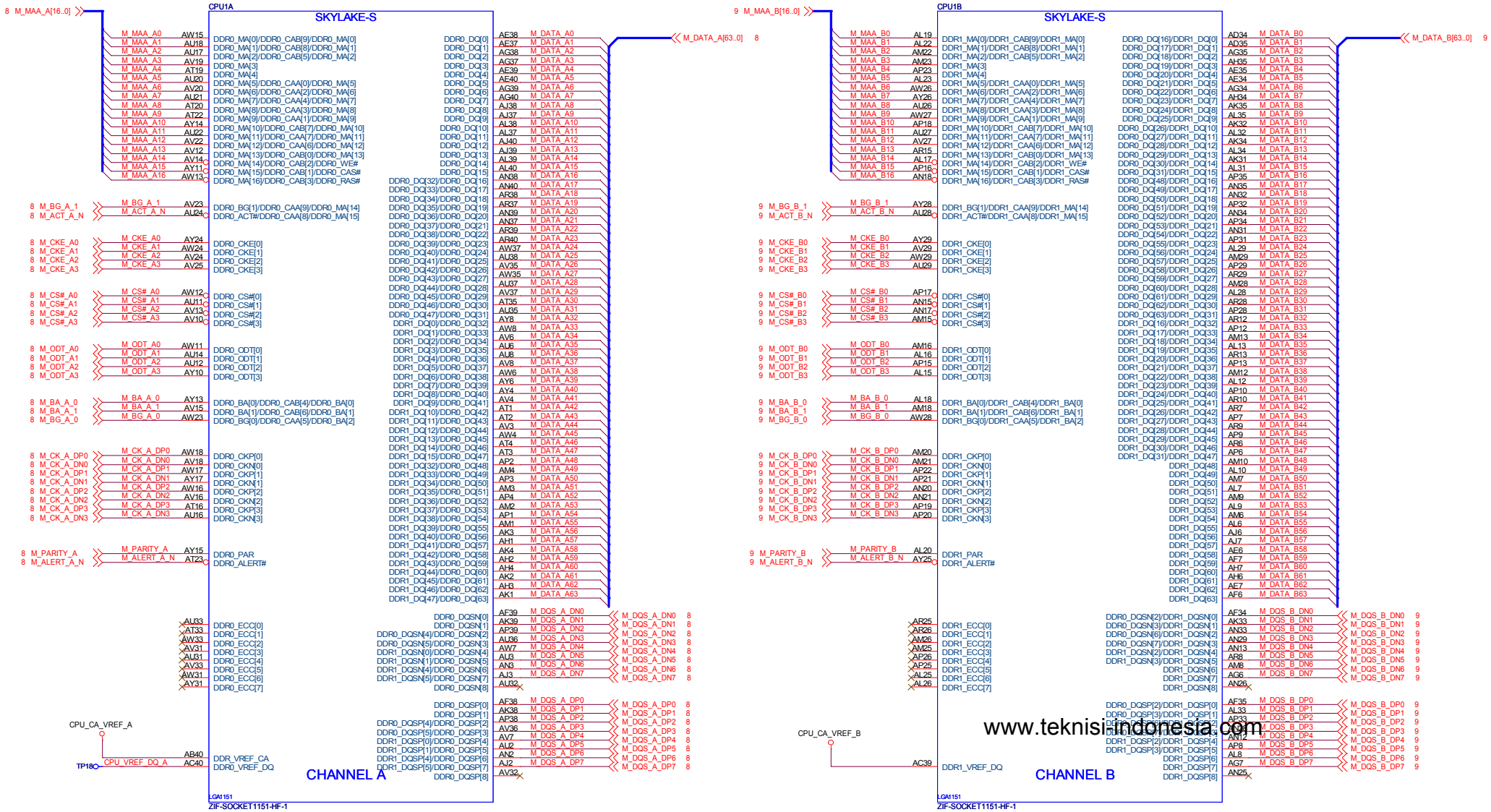
CPU1A
SKYLAKE-S
8 M_MAA_A[16..0]
M_MAA_A0 AW15
M_MAA_A1 AU18
M_MAA_A2 AU17
M_MAA_A3 AY19
M_MAA_A4 AT19
M_MAA_A5 AU20
M_MAA_A6 AV20
M_MAA_A7 AU21
M_MAA_A8 AT20
M_MAA_A9 AT22
M_MAA_A10 AY14
M_MAA_A11 AU22
M_MAA_A12 AV22
M_MAA_A13 AV12
M_MAA_A14 AV14
M_MAA_A15 AY11
M_MAA_A16 AW13
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]
DDR0_MA[3]
DDR0_MA[4]
DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]
DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]
DDR0_MA[14]/DDR0_CAB[2]/DDR0_WE#
DDR0_MA[15]/DDR0_CAB[1]/DDR0_CAS#
DDR0_MA[16]/DDR0_CAB[3]/DDR0_RAS#
8 M_BG_A_1
8 M_ACT_A_N
M_BG_A_1 AV23
M_ACT_A_N AU24
DDR0_BG[1]/DDR0_CAA[9]/DDR0_MA[14]
DDR0_ACT#/DDR0_CAA[8]/DDR0_MA[15]
8 M_CKE_A0
8 M_CKE_A1
8 M_CKE_A2
8 M_CKE_A3
M_CKE_A0 AY24
M_CKE_A1 AW24
M_CKE_A2 AV24
M_CKE_A3 AV25
DDR0_CKE[0]
DDR0_CKE[1]
DDR0_CKE[2]
DDR0_CKE[3]
8 M_CS#_A0
8 M_CS#_A1
8 M_CS#_A2
8 M_CS#_A3
M_CS#_A0 AW12
M_CS#_A1 AU11
M_CS#_A2 AV13
M_CS#_A3 AV10
DDR0_CS#[0]
DDR0_CS#[1]
DDR0_CS#[2]
DDR0_CS#[3]
8 M_ODT_A0
8 M_ODT_A1
8 M_ODT_A2
8 M_ODT_A3
M_ODT_A0 AW11
M_ODT_A1 AU14
M_ODT_A2 AU12
M_ODT_A3 AY10
DDR0_ODT[0]
DDR0_ODT[1]
DDR0_ODT[2]
DDR0_ODT[3]
8 M_BA_A_0
8 M_BA_A_1
8 M_BG_A_0
M_BA_A_0 AY13
M_BA_A_1 AV15
M_BG_A_0 AW23
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]
DDR0_BG[0]/DDR0_CAA[5]/DDR0_BA[2]
8 M_CK_A_DP0
8 M_CK_A_DN0
8 M_CK_A_DP1
8 M_CK_A_DN1
8 M_CK_A_DP2
8 M_CK_A_DN2
8 M_CK_A_DP3
8 M_CK_A_DN3
M_CK_A_DP0 AW18
M_CK_A_DN0 AV18
M_CK_A_DP1 AW17
M_CK_A_DN1 AY17
M_CK_A_DP2 AW16
M_CK_A_DN2 AV16
M_CK_A_DP3 AT16
M_CK_A_DN3 AU16
DDR0_CKP[0]
DDR0_CKN[0]
DDR0_CKP[1]
DDR0_CKN[1]
DDR0_CKP[2]
DDR0_CKN[2]
DDR0_CKP[3]
DDR0_CKN[3]
8 M_PARITY_A
8 M_ALERT_A_N
M_PARITY_A AY15
M_ALERT_A_N AT23
DDR0_PAR
DDR0_ALERT#
AU33 DDR0_ECC[0]
AT33 DDR0_ECC[1]
AW33 DDR0_ECC[2]
AV31 DDR0_ECC[3]
AU31 DDR0_ECC[4]
AV33 DDR0_ECC[5]
AW31 DDR0_ECC[6]
AY31 DDR0_ECC[7]
CPU_CA_VREF_A
AB40 DDR_VREF_CA
TP18 CPU_VREF_DQ_A AC40 DDR0_VREF_DQ
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DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
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DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[32]/DDR0_DQ[16]
DDR0_DQ[33]/DDR0_DQ[17]
DDR0_DQ[34]/DDR0_DQ[18]
DDR0_DQ[35]/DDR0_DQ[19]
DDR0_DQ[36]/DDR0_DQ[20]
DDR0_DQ[37]/DDR0_DQ[21]
DDR0_DQ[38]/DDR0_DQ[22]
DDR0_DQ[39]/DDR0_DQ[23]
DDR0_DQ[40]/DDR0_DQ[24]
DDR0_DQ[41]/DDR0_DQ[25]
DDR0_DQ[42]/DDR0_DQ[26]
DDR0_DQ[43]/DDR0_DQ[27]
DDR0_DQ[44]/DDR0_DQ[28]
DDR0_DQ[45]/DDR0_DQ[29]
DDR0_DQ[46]/DDR0_DQ[30]
DDR0_DQ[47]/DDR0_DQ[31]
DDR1_DQ[0]/DDR0_DQ[32]
DDR1_DQ[1]/DDR0_DQ[33]
DDR1_DQ[2]/DDR0_DQ[34]
DDR1_DQ[3]/DDR0_DQ[35]
DDR1_DQ[4]/DDR0_DQ[36]
DDR1_DQ[5]/DDR0_DQ[37]
DDR1_DQ[6]/DDR0_DQ[38]
DDR1_DQ[7]/DDR0_DQ[39]
DDR1_DQ[8]/DDR0_DQ[40]
DDR1_DQ[9]/DDR0_DQ[41]
DDR1_DQ[10]/DDR0_DQ[42]
DDR1_DQ[11]/DDR0_DQ[43]
DDR1_DQ[12]/DDR0_DQ[44]
DDR1_DQ[13]/DDR0_DQ[45]
DDR1_DQ[14]/DDR0_DQ[46]
DDR1_DQ[15]/DDR0_DQ[47]
DDR1_DQ[32]/DDR0_DQ[48]
DDR1_DQ[33]/DDR0_DQ[49]
DDR1_DQ[34]/DDR0_DQ[50]
DDR1_DQ[35]/DDR0_DQ[51]
DDR1_DQ[36]/DDR0_DQ[52]
DDR1_DQ[37]/DDR0_DQ[53]
DDR1_DQ[38]/DDR0_DQ[54]
DDR1_DQ[39]/DDR0_DQ[55]
DDR1_DQ[40]/DDR0_DQ[56]
DDR1_DQ[41]/DDR0_DQ[57]
DDR1_DQ[42]/DDR0_DQ[58]
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DDR1_DQ[46]/DDR0_DQ[62]
DDR1_DQ[47]/DDR0_DQ[63]
AE38 M_DATA_A0
AE37 M_DATA_A1
AG38 M_DATA_A2
AG37 M_DATA_A3
AE39 M_DATA_A4
AE40 M_DATA_A5
AG39 M_DATA_A6
AG40 M_DATA_A7
AJ38 M_DATA_A8
AJ37 M_DATA_A9
AL38 M_DATA_A10
AL37 M_DATA_A11
AJ40 M_DATA_A12
AJ39 M_DATA_A13
AL39 M_DATA_A14
AL40 M_DATA_A15
AN38 M_DATA_A16
AN40 M_DATA_A17
AR38 M_DATA_A18
AR37 M_DATA_A19
AN39 M_DATA_A20
AN37 M_DATA_A21
AR39 M_DATA_A22
AR40 M_DATA_A23
AW37 M_DATA_A24
AU38 M_DATA_A25
AV35 M_DATA_A26
AW35 M_DATA_A27
AU37 M_DATA_A28
AV37 M_DATA_A29
AT35 M_DATA_A30
AU35 M_DATA_A31
AY8 M_DATA_A32
AW8 M_DATA_A33
AV6 M_DATA_A34
AU6 M_DATA_A35
AU8 M_DATA_A36
AV8 M_DATA_A37
AW6 M_DATA_A38
AY6 M_DATA_A39
AY4 M_DATA_A40
AV4 M_DATA_A41
AT1 M_DATA_A42
AT2 M_DATA_A43
AV3 M_DATA_A44
AW4 M_DATA_A45
AT4 M_DATA_A46
AT3 M_DATA_A47
AP2 M_DATA_A48
AM4 M_DATA_A49
AP3 M_DATA_A50
AM3 M_DATA_A51
AP4 M_DATA_A52
AM2 M_DATA_A53
AP1 M_DATA_A54
AM1 M_DATA_A55
AK3 M_DATA_A56
AH1 M_DATA_A57
AK4 M_DATA_A58
AH2 M_DATA_A59
AH4 M_DATA_A60
AK2 M_DATA_A61
AH3 M_DATA_A62
AK1 M_DATA_A63
M_DATA_A[63..0] 8
AF39 M_DQS_A_DN0
AK39 M_DQS_A_DN1
AP39 M_DQS_A_DN2
AU36 M_DQS_A_DN3
AW7 M_DQS_A_DN4
AU3 M_DQS_A_DN5
AN3 M_DQS_A_DN6
AJ3 M_DQS_A_DN7
AU32
M_DQS_A_DN0 8
M_DQS_A_DN1 8
M_DQS_A_DN2 8
M_DQS_A_DN3 8
M_DQS_A_DN4 8
M_DQS_A_DN5 8
M_DQS_A_DN6 8
M_DQS_A_DN7 8
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DDR0_DQSN[1]
DDR0_DQSN[4]/DDR0_DQSN[2]
DDR0_DQSN[5]/DDR0_DQSN[3]
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DDR1_DQSN[1]/DDR0_DQSN[5]
DDR1_DQSN[4]/DDR0_DQSN[6]
DDR1_DQSN[5]/DDR0_DQSN[7]
DDR0_DQSN[8]
AF38 M_DQS_A_DP0
AK38 M_DQS_A_DP1
AP38 M_DQS_A_DP2
AV36 M_DQS_A_DP3
AV7 M_DQS_A_DP4
AU2 M_DQS_A_DP5
AN2 M_DQS_A_DP6
AJ2 M_DQS_A_DP7
AV32
M_DQS_A_DP0 8
M_DQS_A_DP1 8
M_DQS_A_DP2 8
M_DQS_A_DP3 8
M_DQS_A_DP4 8
M_DQS_A_DP5 8
M_DQS_A_DP6 8
M_DQS_A_DP7 8
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DDR1_DQSP[1]/DDR0_DQSP[5]
DDR1_DQSP[4]/DDR0_DQSP[6]
DDR1_DQSP[5]/DDR0_DQSP[7]
DDR0_DQSP[8]
CHANNEL A
LGA1151
ZIF-SOCKET1151-HF-1
CPU1B
SKYLAKE-S
9 M_MAA_B[16..0]
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M_MAA_B1 AL22
M_MAA_B2 AM22
M_MAA_B3 AM23
M_MAA_B4 AP23
M_MAA_B5 AL23
M_MAA_B6 AW26
M_MAA_B7 AY26
M_MAA_B8 AU26
M_MAA_B9 AW27
M_MAA_B10 AP18
M_MAA_B11 AU27
M_MAA_B12 AV27
M_MAA_B13 AR15
M_MAA_B14 AL17
M_MAA_B15 AP16
M_MAA_B16 AN18
DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]
DDR1_MA[3]
DDR1_MA[4]
DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
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DDR1_MA[14]/DDR1_CAB[2]/DDR1_WE#
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9 M_BG_B_1
9 M_ACT_B_N
M_BG_B_1 AY28
M_ACT_B_N AU28
DDR1_BG[1]/DDR1_CAA[9]/DDR1_MA[14]
DDR1_ACT#/DDR1_CAA[8]/DDR1_MA[15]
9 M_CKE_B0
9 M_CKE_B1
9 M_CKE_B2
9 M_CKE_B3
M_CKE_B0 AY29
M_CKE_B1 AL29
M_CKE_B2 AW29
M_CKE_B3 AU29
DDR1_CKE[0]
DDR1_CKE[1]
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9 M_CS#_B0
9 M_CS#_B1
9 M_CS#_B2
9 M_CS#_B3
M_CS#_B0 AP17
M_CS#_B1 AN15
M_CS#_B2 AN17
M_CS#_B3 AM15
DDR1_CS#[0]
DDR1_CS#[1]
DDR1_CS#[2]
DDR1_CS#[3]
9 M_ODT_B0
9 M_ODT_B1
9 M_ODT_B2
9 M_ODT_B3
M_ODT_B0 AM16
M_ODT_B1 AL16
M_ODT_B2 AP15
M_ODT_B3 AL15
DDR1_ODT[0]
DDR1_ODT[1]
DDR1_ODT[2]
DDR1_ODT[3]
9 M_BA_B_0
9 M_BA_B_1
9 M_BG_B_0
M_BA_B_0 AL18
M_BA_B_1 AM18
M_BG_B_0 AW28
DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_BG[0]/DDR1_CAA[5]/DDR1_BA[2]
9 M_CK_B_DP0
9 M_CK_B_DN0
9 M_CK_B_DP1
9 M_CK_B_DN1
9 M_CK_B_DP2
9 M_CK_B_DN2
9 M_CK_B_DP3
9 M_CK_B_DN3
M_CK_B_DP0 AM20
M_CK_B_DN0 AM21
M_CK_B_DP1 AP22
M_CK_B_DN1 AP21
M_CK_B_DP2 AN20
M_CK_B_DN2 AN21
M_CK_B_DP3 AP19
M_CK_B_DN3 AP20
DDR1_CKP[0]
DDR1_CKN[0]
DDR1_CKP[1]
DDR1_CKN[1]
DDR1_CKP[2]
DDR1_CKN[2]
DDR1_CKP[3]
DDR1_CKN[3]
9 M_PARITY_B
9 M_ALERT_B_N
M_PARITY_B AL20
M_ALERT_B_N AY25
DDR1_PAR
DDR1_ALERT#
AR25 DDR1_ECC[0]
AR26 DDR1_ECC[1]
AM26 DDR1_ECC[2]
AM25 DDR1_ECC[3]
AP26 DDR1_ECC[4]
AP25 DDR1_ECC[5]
AL25 DDR1_ECC[6]
AL26 DDR1_ECC[7]
CPU_CA_VREF_B
AC39 DDR1_VREF_DQ
DDR0_DQ[16]/DDR1_DQ[0]
DDR0_DQ[17]/DDR1_DQ[1]
DDR0_DQ[18]/DDR1_DQ[2]
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DDR1_DQ[59]
DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]
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AD35 M_DATA_B1
AG35 M_DATA_B2
AH35 M_DATA_B3
AE35 M_DATA_B4
AE34 M_DATA_B5
AG34 M_DATA_B6
AH34 M_DATA_B7
AK35 M_DATA_B8
AL35 M_DATA_B9
AK32 M_DATA_B10
AL32 M_DATA_B11
AK34 M_DATA_B12
AL34 M_DATA_B13
AK31 M_DATA_B14
AL31 M_DATA_B15
AP35 M_DATA_B16
AN35 M_DATA_B17
AN32 M_DATA_B18
AP32 M_DATA_B19
AN34 M_DATA_B20
AP34 M_DATA_B21
AN31 M_DATA_B22
AP31 M_DATA_B23
AL29 M_DATA_B24
AM29 M_DATA_B25
AP29 M_DATA_B26
AR29 M_DATA_B27
AM28 M_DATA_B28
AL28 M_DATA_B29
AR28 M_DATA_B30
AP28 M_DATA_B31
AR12 M_DATA_B32
AP12 M_DATA_B33
AM13 M_DATA_B34
AL13 M_DATA_B35
AR13 M_DATA_B36
AP13 M_DATA_B37
AM12 M_DATA_B38
AL12 M_DATA_B39
AP10 M_DATA_B40
AR10 M_DATA_B41
AR7 M_DATA_B42
AP7 M_DATA_B43
AR9 M_DATA_B44
AP9 M_DATA_B45
AR6 M_DATA_B46
AP6 M_DATA_B47
AM10 M_DATA_B48
AL10 M_DATA_B49
AM7 M_DATA_B50
AL7 M_DATA_B51
AM9 M_DATA_B52
AL9 M_DATA_B53
AM6 M_DATA_B54
AL6 M_DATA_B55
AJ6 M_DATA_B56
AJ7 M_DATA_B57
AF6 M_DATA_B58
AF7 M_DATA_B59
AH7 M_DATA_B60
AH6 M_DATA_B61
AE7 M_DATA_B62
AF6 M_DATA_B63
M_DATA_B[63..0] 9
AF34 M_DQS_B_DN0
AK33 M_DQS_B_DN1
AN33 M_DQS_B_DN2
AP29 M_DQS_B_DN3
AN13 M_DQS_B_DN4
AR8 M_DQS_B_DN5
AM8 M_DQS_B_DN6
AG6 M_DQS_B_DN7
AN26
M_DQS_B_DN0 9
M_DQS_B_DN1 9
M_DQS_B_DN2 9
M_DQS_B_DN3 9
M_DQS_B_DN4 9
M_DQS_B_DN5 9
M_DQS_B_DN6 9
M_DQS_B_DN7 9
DDR0_DQSN[2]/DDR1_DQSN[0]
DDR0_DQSN[3]/DDR1_DQSN[1]
DDR0_DQSN[6]/DDR1_DQSN[2]
DDR0_DQSN[7]/DDR1_DQSN[3]
DDR1_DQSN[2]/DDR1_DQSN[4]
DDR1_DQSN[3]/DDR1_DQSN[5]
DDR1_DQSN[6]
DDR1_DQSN[7]
DDR1_DQSN[8]
AF35 M_DQS_B_DP0
AL33 M_DQS_B_DP1
AP33 M_DQS_B_DP2
AN29 M_DQS_B_DP3
AN12 M_DQS_B_DP4
AP8 M_DQS_B_DP5
AL8 M_DQS_B_DP6
AG7 M_DQS_B_DP7
AN25
M_DQS_B_DP0 9
M_DQS_B_DP1 9
M_DQS_B_DP2 9
M_DQS_B_DP3 9
M_DQS_B_DP4 9
M_DQS_B_DP5 9
M_DQS_B_DP6 9
M_DQS_B_DP7 9
DDR0_DQSP[2]/DDR1_DQSP[0]
DDR0_DQSP[3]/DDR1_DQSP[1]
DDR0_DQSP[6]/DDR1_DQSP[2]
DDR0_DQSP[7]/DDR1_DQSP[3]
DDR1_DQSP[2]/DDR1_DQSP[4]
DDR1_DQSP[3]/DDR1_DQSP[5]
DDR1_DQSP[6]
DDR1_DQSP[7]
DDR1_DQSP[8]
CHANNEL B
LGA1151
ZIF-SOCKET1151-HF-1
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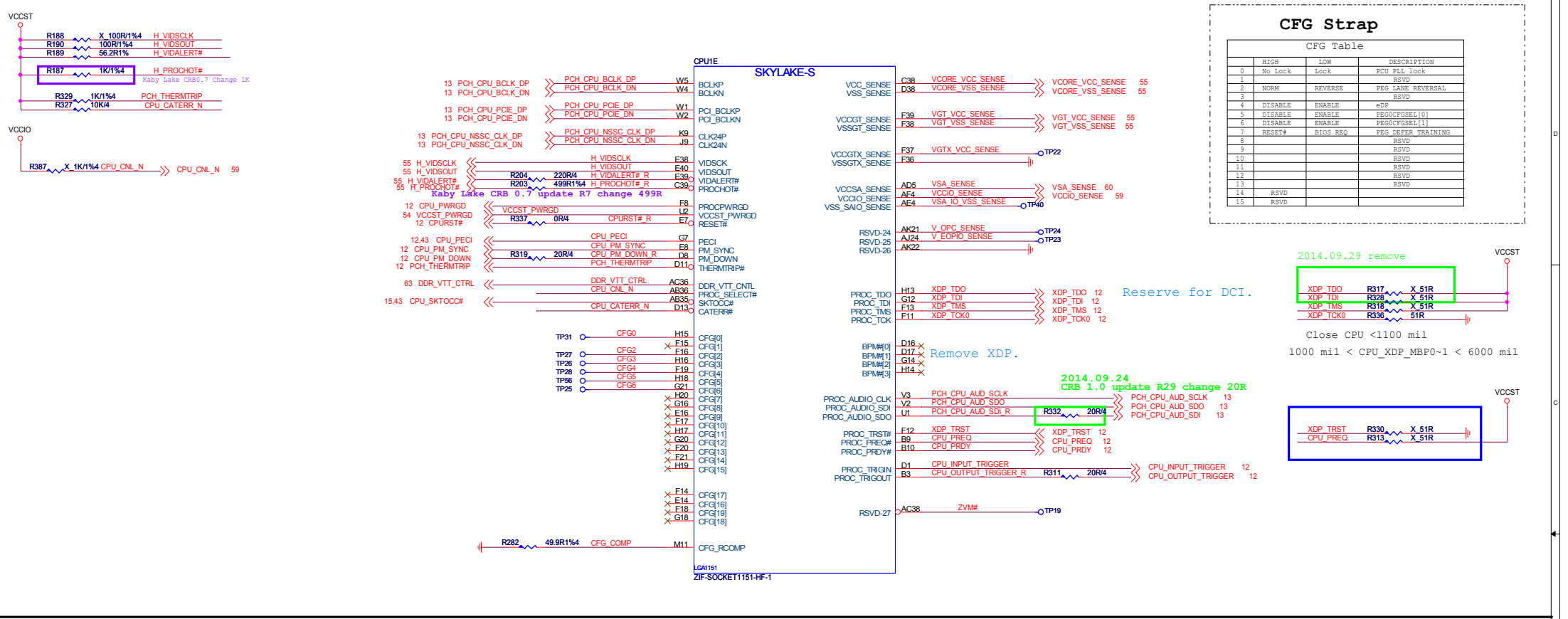
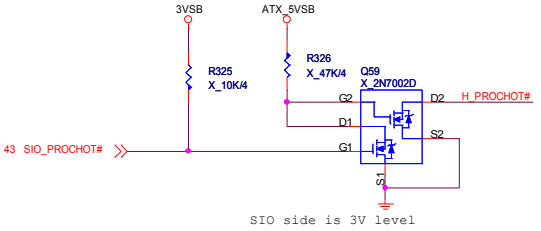
MICRO-STAR INT'L CO.,LTD
MS-7A64..
Size Custom
Document Description CPU-Memory
Rev 10
Date: Tuesday, September 20, 2016
Sheet 3 of 69



CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU_PLL_lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		



CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU_PLL_lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG_DEFER_TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		

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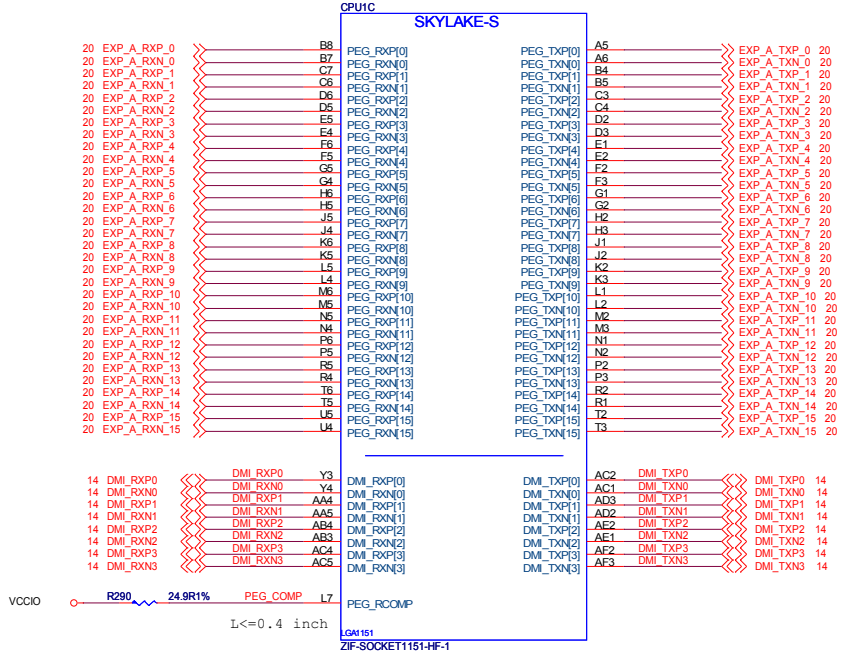
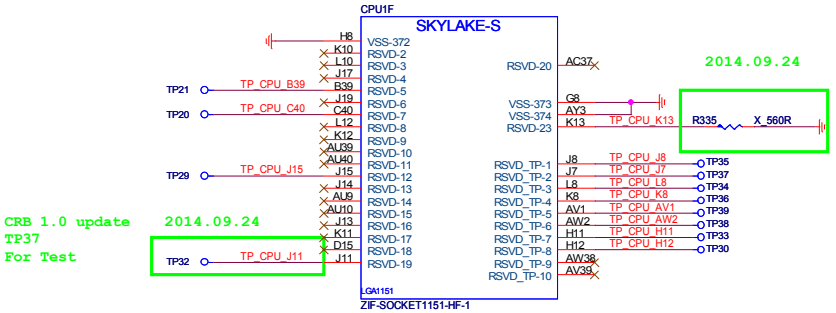
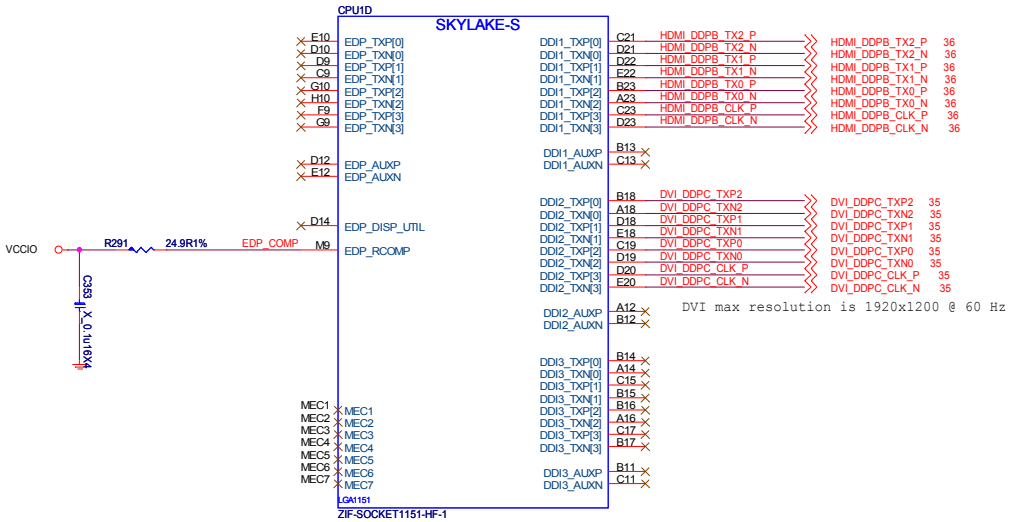
MS-7A64..

Size: Custom | Document Description: CPU-Control/MISC/CFG/Audio | Rev: 10

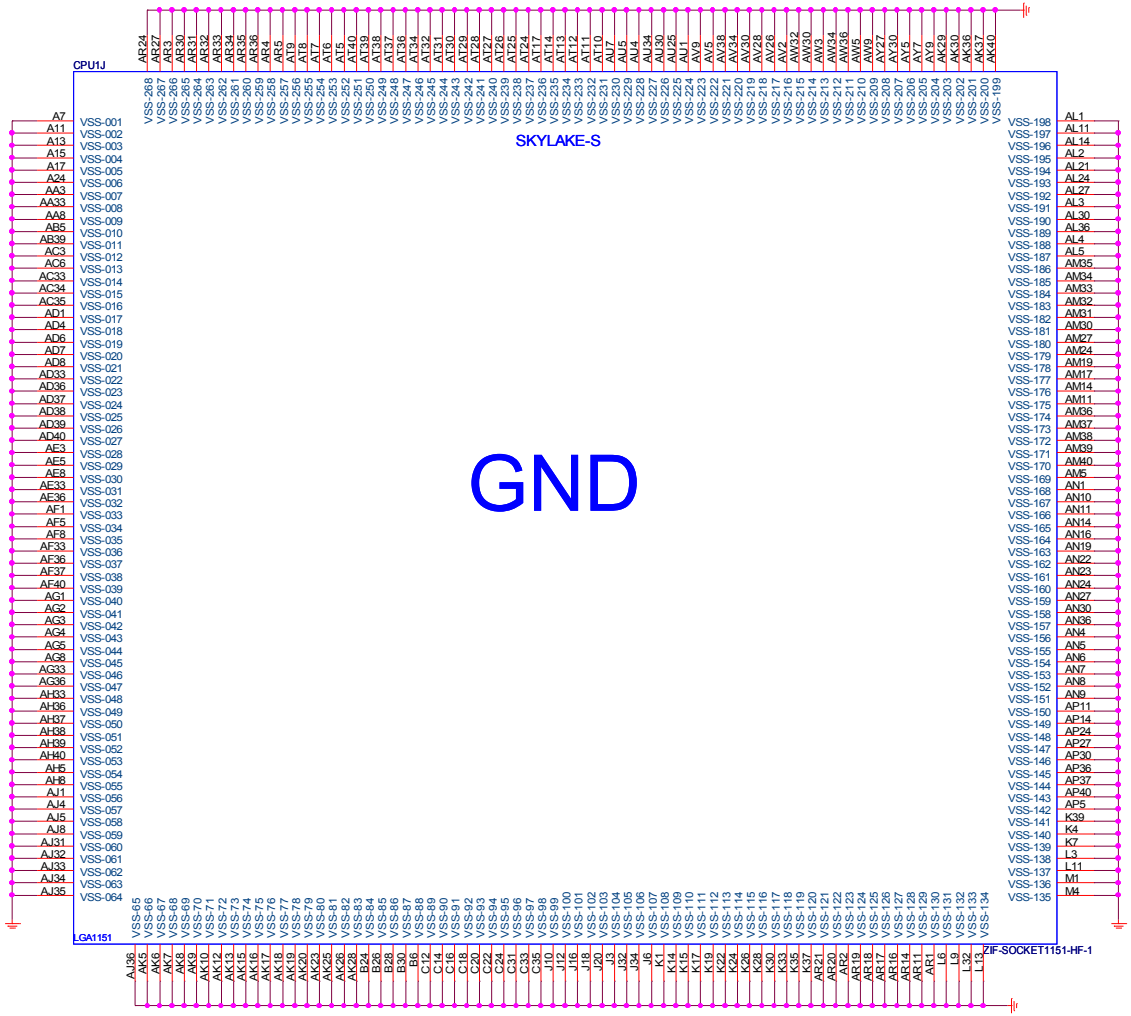
Date: Wednesday, September 21, 2016 | Sheet 4 of 69

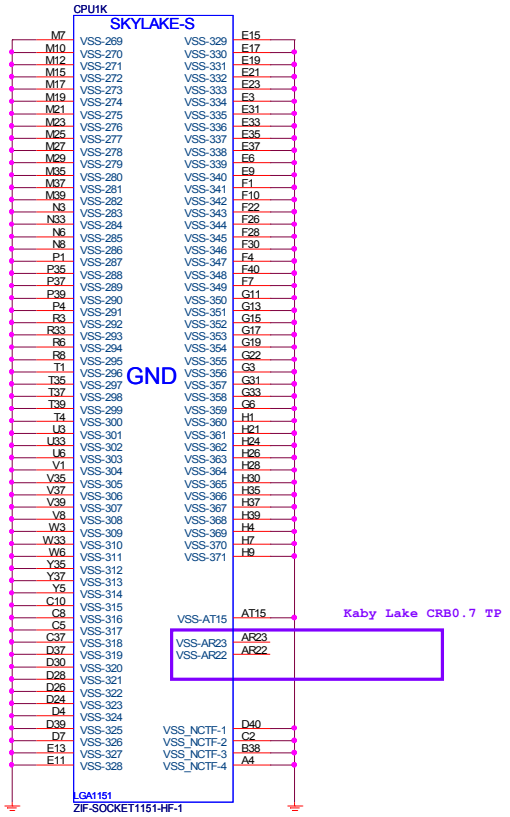




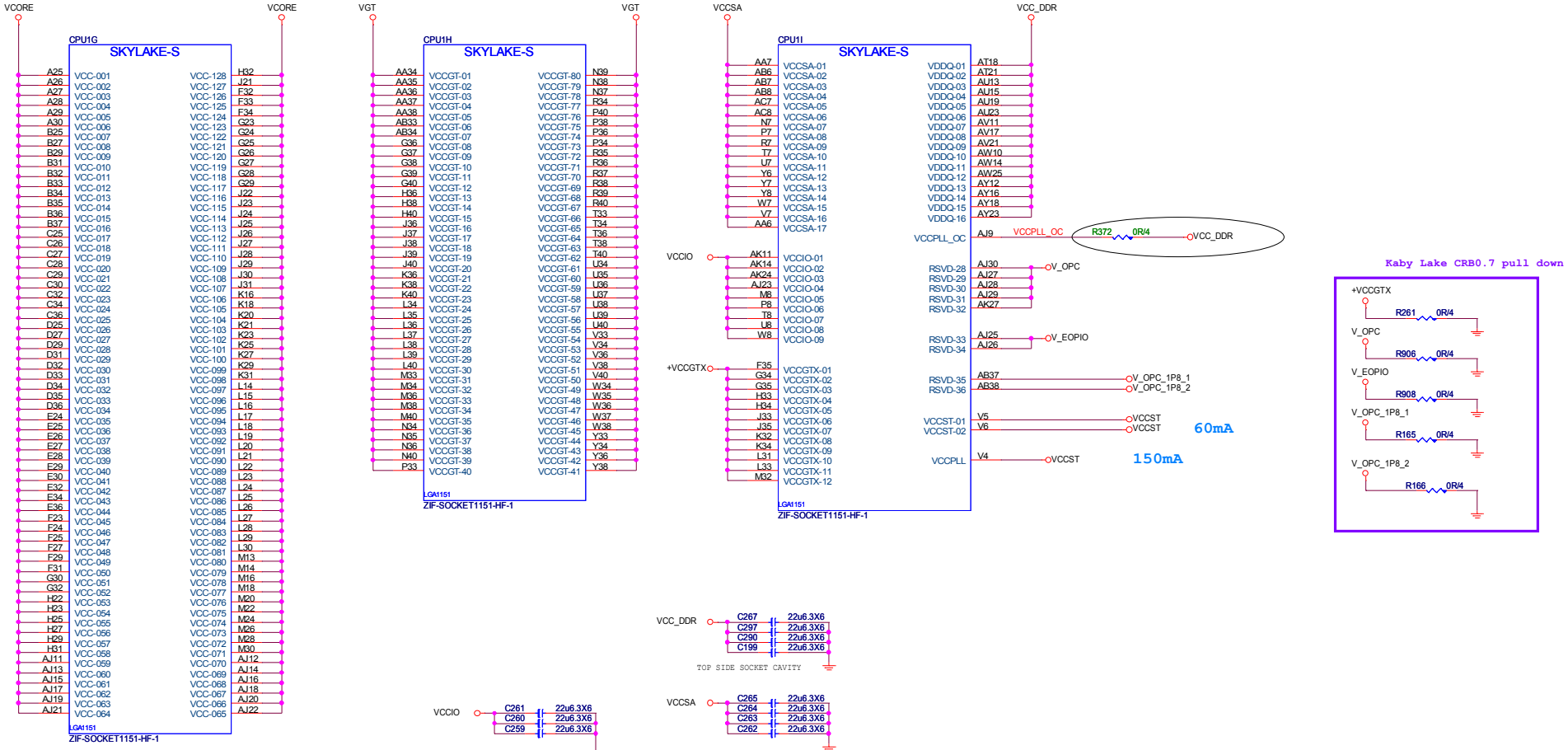


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
Size: Custom	Document Description: CPU-PEG/Display	Rev: 10
Date: Tuesday, September 20, 2016	Sheet 5 of 69	

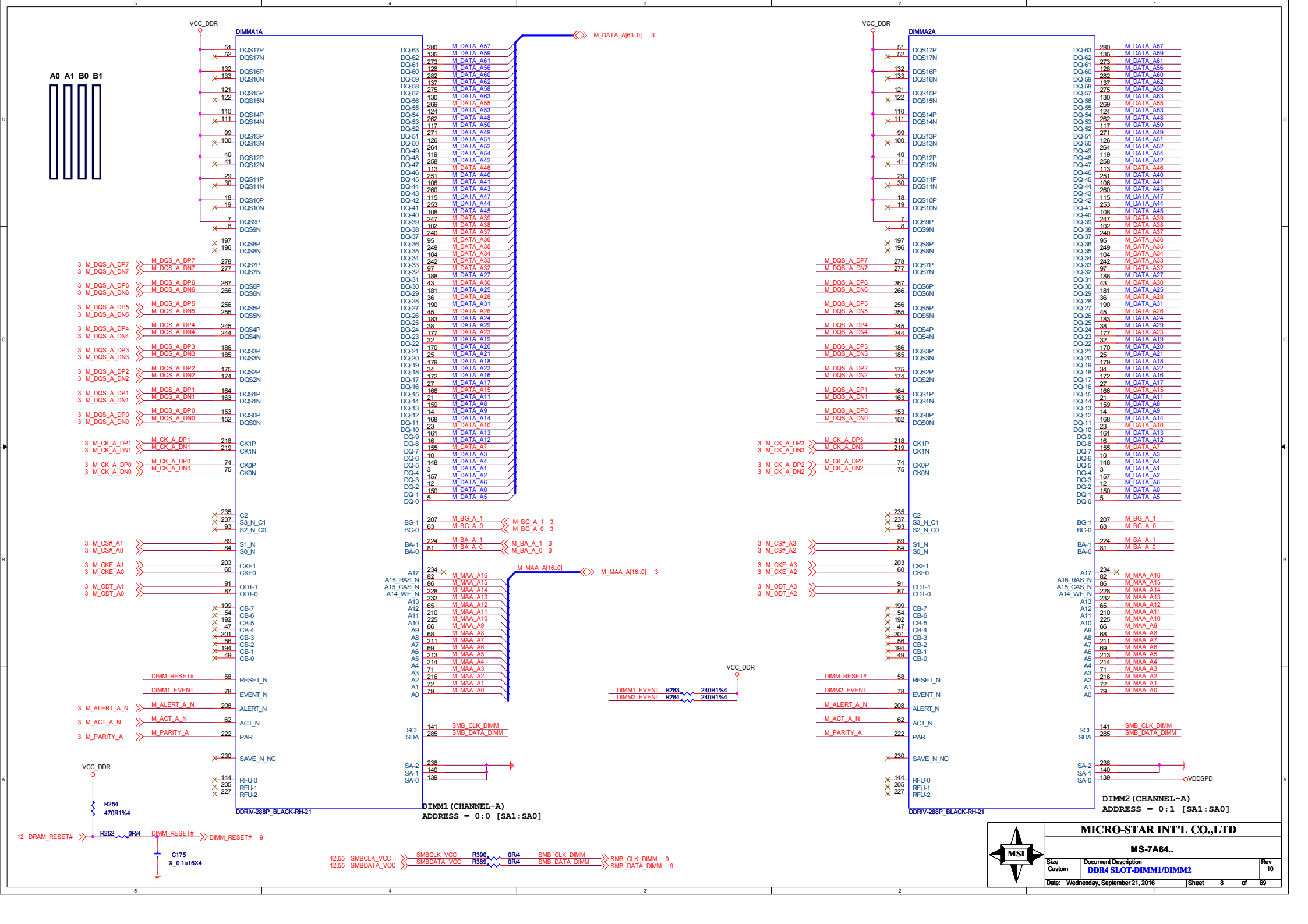


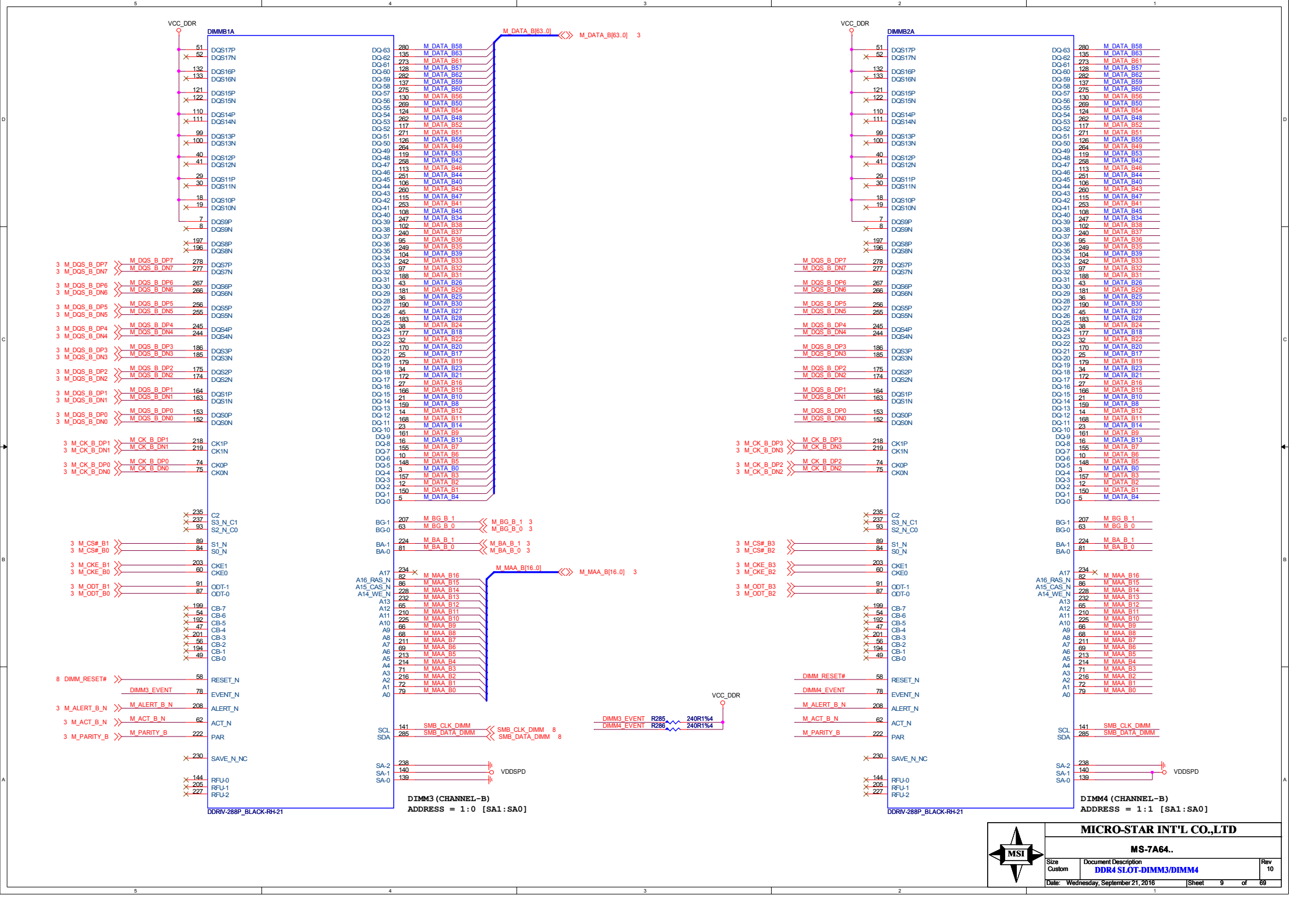


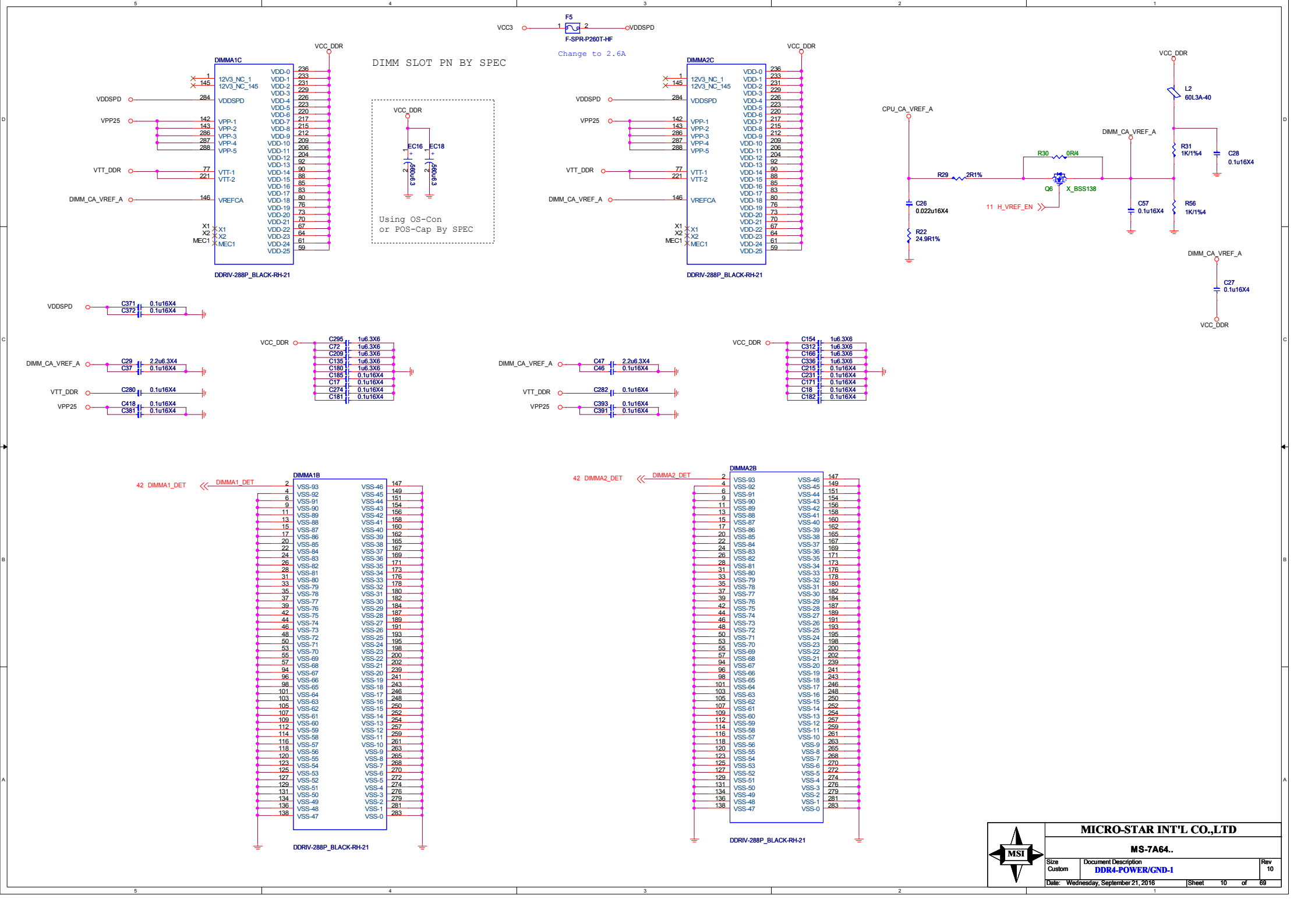
MICRO-STAR INT'L CO.,LTD			
MS-7A64..			
Size: Custom	Document Description: CPU-GND		Rev: 10
Date: Wednesday, September 21, 2016		Sheet 6 of 69	



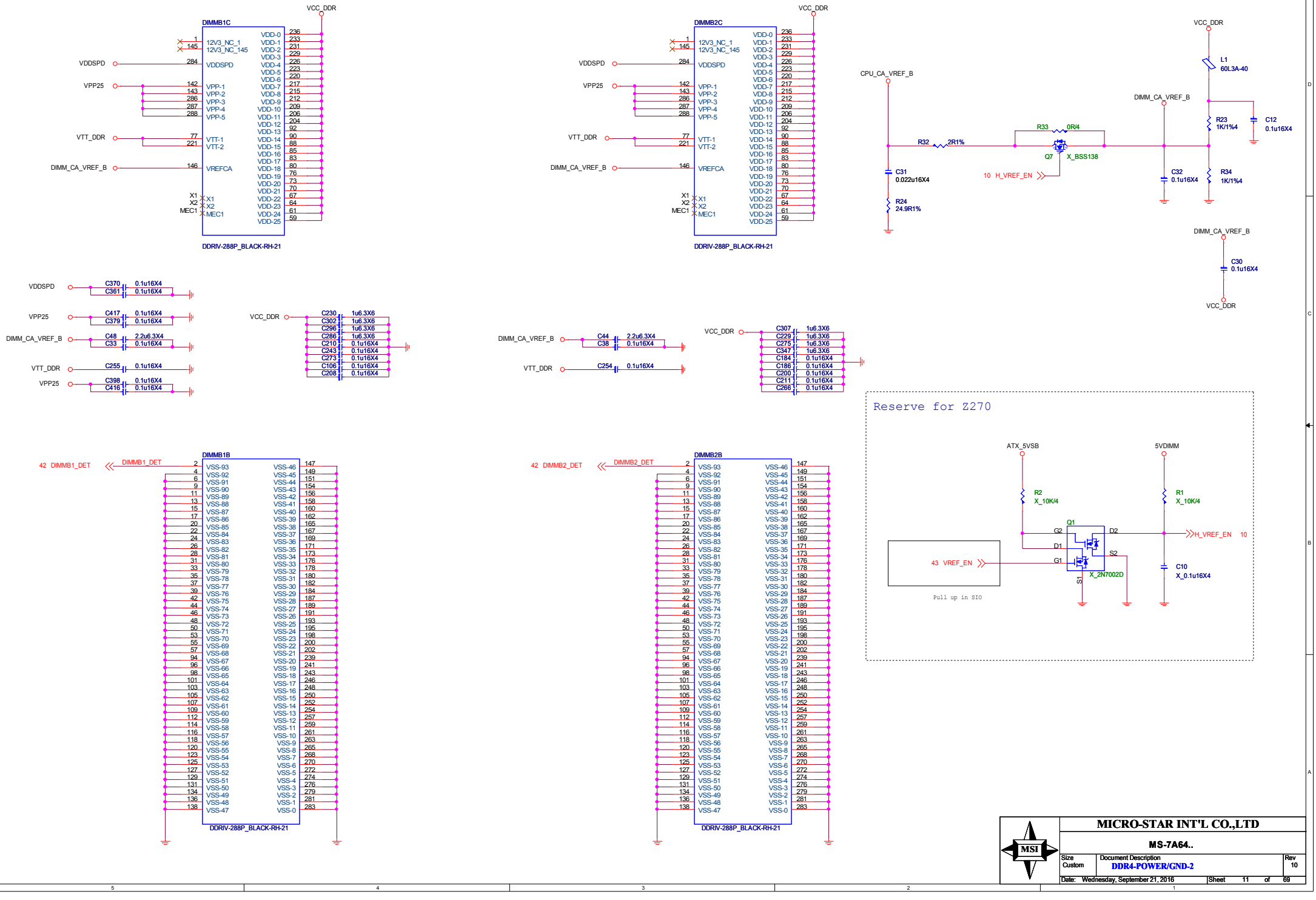
MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: CPU-Power
Rev: 10	
Date: Wednesday, September 21, 2016	Sheet 7 of 69


A0 A1 B0 B1
VCC_DDR
DIMMA1A
DDRIV-288P_BLACK-RH-21
DIMM1 (CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
VCC_DDR
DIMMA2A
DDRIV-288P_BLACK-RH-21
DIMM2 (CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
VCC_DDR
R254
470R1%4
12 DRAM_RESET#
R252 0R/4
DIMM_RESET#
DIMM_RESET# 9
C175
X_0.1u16X4
12,55 SMBCLK_VCC
12,55 SMBDATA_VCC
SMBCLK_VCC
SMBDATA_VCC
R390 0R/4
R389 0R/4
SMB_CLK_DIMM
SMB_DATA_DIMM
SMB_CLK_DIMM 9
SMB_DATA_DIMM 9
VCC_DDR
DIMM1_EVENT R283 240R1%4
DIMM2_EVENT R284 240R1%4
VDDSPD
MICRO-STAR INT'L CO.,LTD
MS-7A64..
Size Custom
Document Description
DDR4 SLOT-DIMM1/DIMM2
Rev 10
Date: Wednesday, September 21, 2016
Sheet 8 of 69

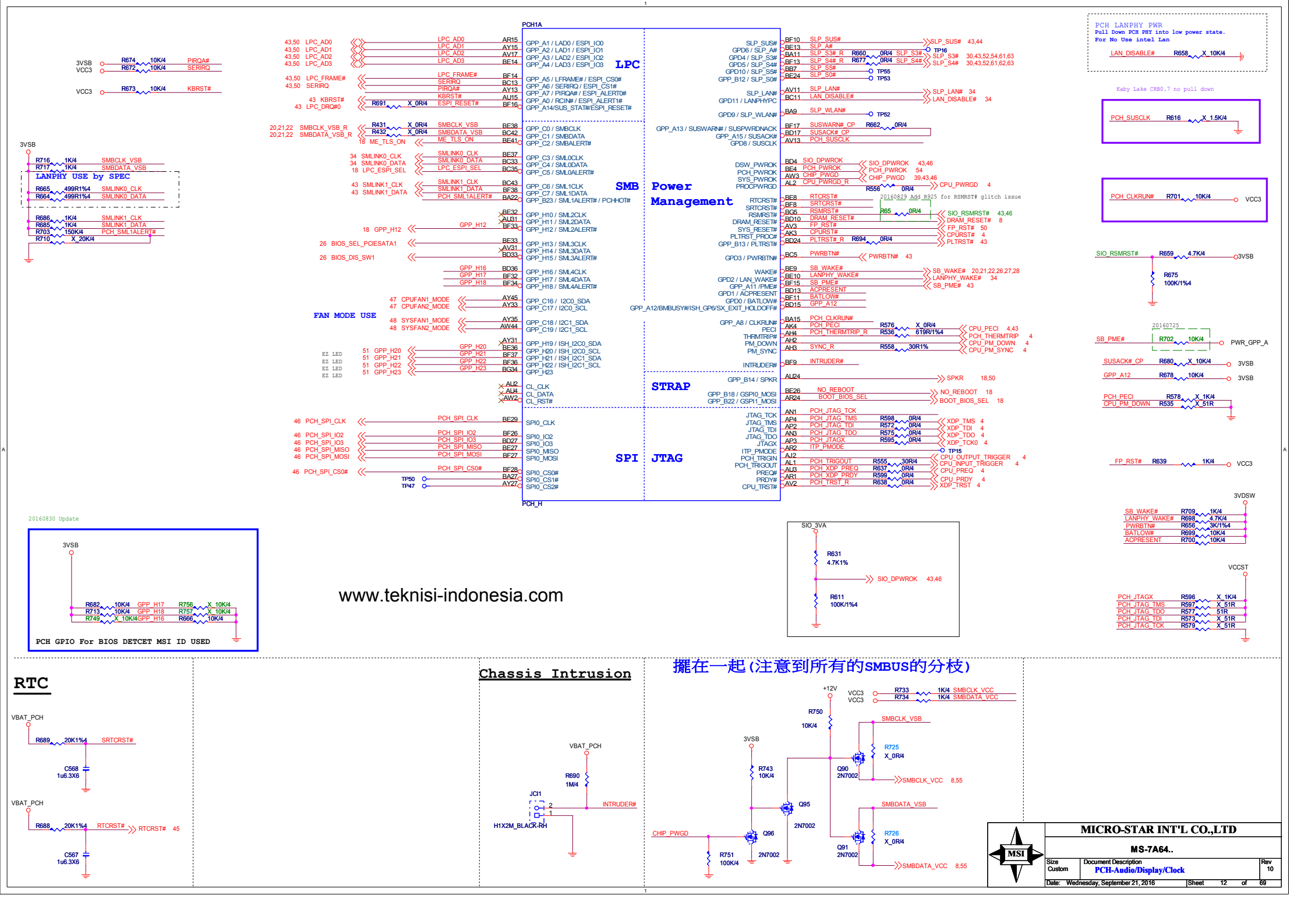

DIMMB1A
DDRIV-288P_BLACK-RH-21
DIMM3 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]
DIMMB2A
DDRIV-288P_BLACK-RH-21
DIMM4 (CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]
VCC_DDR
VDDSPD
M_DATA_B[63..0]
M_MAA_B[16..0]
DIMM3_EVENT R285 240R1%4
DIMM4_EVENT R286 240R1%4
MICRO-STAR INT'L CO.,LTD
MS-7A64..
Size Custom
Document Description
DDR4 SLOT-DIMM3/DIMM4
Rev 10
Date: Wednesday, September 21, 2016
Sheet 9 of 69



MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: DDR4-POWER/GND-1	Rev: 10
Date: Wednesday, September 21, 2016	Sheet 10 of 69	



MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: DDR4-POWER/GND-2	Rev: 10
Date: Wednesday, September 21, 2016	Sheet 11 of 69	


PCH1A
LPC
SMB
Power Management
STRAP
JTAG
SPI
FAN MODE USE
LANPHY USE by SPEC
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
Kaby Lake CRB0.7 no pull down
20160830 Update
PCH GPIO For BIOS DETCET MSI ID USED
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RTC
Chassis Intrusion
擺在一起(注意到所有的SMBUS的分枝)
MICRO-STAR INT'L CO.,LTD
MS-7A64..
PCH-Audio/Display/Clock
Date: Wednesday, September 21, 2016
Sheet 12 of 69

PCH_CLK

RTC Block

Close to PCH

C607 12p50N6 — RTCX2
Y2
R697 10M/6 <1 inch
C581 12p50N6 — RTCX1
32.768KHZ12.5p_D-RH-10

VCC3

R704	10K/4	LAN_CLKREQ#4
R803	10K/4	ASM1083_CLKREQ#7
R707	10K/4	M2_CLKREQ#9
R706	10K/4	M2_CLKREQ#10
R705	10K/4	ASM1142_CLKREQ#5

EMI
CLK_SIO_PCI — C598 X_10p50N4
TPM_CLK — C599 X_10p50N4

XTAL_24M_PCH_OUT_R — R478 0R/4 — XTAL_24M_PCH_OUT
R480 1M/1%4
XTAL_24M_PCH_IN_R — R479 0R/4 — XTAL_24M_PCH_IN
Y1
24MHZ20p_S-HF
C495 22p50N4
C502 22p50N4

PCH1E

43 CLK_SIO_PCI	R661 22R/4	CLK_PCH_LPC0	BE15	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK
50 TPM_CLK	R679 22R/4	CLK_PCH_LPC1	AY17	GPP_A10 / CLKOUT_LPC1
			BC17	GPP_A16 / CLKOUT_48

LPC

RTCX1	BF7	RTCX1
RTCX2	BG7	RTCX2

RTC

XTAL_24M_PCH_IN	E1	XTAL24_IN
XTAL_24M_PCH_OUT	A5	XTAL24_OUT
PCH_CLK5_1P0 — C526 0.1u16X4 — R491 2.7K1% XCLK_BIASREF	F1	XCLK_BIASREF

24MHZ

XCLK_BIASREF < 500 mil

CLK_REQ

LAN	34 LAN_CLKREQ#4	LAN_CLKREQ#4	BE22	GPP_B5 / SRCCLKREQ0#
ASMEDIA1142	28 ASM1142_CLKREQ#5	ASM1142_CLKREQ#5	BA24	GPP_B6 / SRCCLKREQ1#
			BA19	GPP_B7 / SRCCLKREQ2#
			BF23	GPP_B8 / SRCCLKREQ3#
			BD22	GPP_B9 / SRCCLKREQ4#
			BF24	GPP_B10 / SRCCLKREQ5#
ASMEDIA1083	23 ASM1083_CLKREQ#7	ASM1083_CLKREQ#7	AR29	GPP_H0 / SRCCLKREQ6#
M.2	26 M2_CLKREQ#9	M2_CLKREQ#9	AU27	GPP_H1 / SRCCLKREQ7#
	27 M2_CLKREQ#10	M2_CLKREQ#10	BG30	GPP_H2 / SRCCLKREQ8#
			BF30	GPP_H3 / SRCCLKREQ9#
			BD29	GPP_H4 / SRCCLKREQ10#
			BE31	GPP_H5 / SRCCLKREQ11#
			AY29	GPP_H6 / SRCCLKREQ12#
			AV29	GPP_H7 / SRCCLKREQ13#
			BD31	GPP_H8 / SRCCLKREQ14#
			BF31	GPP_H9 / SRCCLKREQ15#

PCH_H

CLKOUT_CPUBCLK_P	H1	PCH_CPU_BCLK_DP	PCH_CPU_BCLK_DP 4
CLKOUT_CPUBCLK_N	H2	PCH_CPU_BCLK_DN	PCH_CPU_BCLK_DN 4
CLKOUT_CPUNSSC_P	G2	PCH_CPU_NSSC_CLK_DP	PCH_CPU_NSSC_CLK_DP 4
CLKOUT_CPUNSSC_N	G1	PCH_CPU_NSSC_CLK_DN	PCH_CPU_NSSC_CLK_DN 4
CLKOUT_CPUPCIBCLK_P	J2	PCH_CPU_PCIE_DP	PCH_CPU_PCIE_DP 4
CLKOUT_CPUPCIBCLK_N	J3	PCH_CPU_PCIE_DN	PCH_CPU_PCIE_DN 4
CLKOUT_ITPXDP_P	L3		
CLKOUT_ITPXDP_N	L2		
CLKOUT_PCIE_P0	P7	CLK_PE2_DP	CLK_PE2_DP 22
CLKOUT_PCIE_N0	P5	CLK_PE2_DN	CLK_PE2_DN 22
CLKOUT_PCIE_P1	M5		
CLKOUT_PCIE_N1	M7		
CLKOUT_PCIE_P2	G7	CLK_PE4_DP	CLK_PE4_DP 21
CLKOUT_PCIE_N2	H7	CLK_PE4_DN	CLK_PE4_DN 21
CLKOUT_PCIE_P3	K5	CLK_PE1_DP	CLK_PE1_DP 20
CLKOUT_PCIE_N3	K7	CLK_PE1_DN	CLK_PE1_DN 20
CLKOUT_PCIE_P4	E4	CLK_LAN_DP	CLK_LAN_DP 34
CLKOUT_PCIE_N4	E3	CLK_LAN_DN	CLK_LAN_DN 34
CLKOUT_PCIE_P5	C6	CLK_ASM1142_DP	CLK_ASM1142_DP 28
CLKOUT_PCIE_N5	C5	CLK_ASM1142_DN	CLK_ASM1142_DN 28
CLKOUT_PCIE_P6	T7	CLK_PE3_DP	CLK_PE3_DP 22
CLKOUT_PCIE_N6	T8	CLK_PE3_DN	CLK_PE3_DN 22
CLKOUT_PCIE_P7	V7	CLK_ASM1083_DP	CLK_ASM1083_DP 23
CLKOUT_PCIE_N7	V5	CLK_ASM1083_DN	CLK_ASM1083_DN 23
CLKOUT_PCIE_P8	Y11		
CLKOUT_PCIE_N8	Y10		
CLKOUT_PCIE_P9	M1	CLK_M2_1_DP	CLK_M2_1_DP 26
CLKOUT_PCIE_N9	M2	CLK_M2_1_DN	CLK_M2_1_DN 26
CLKOUT_PCIE_P10	P2	CLK_M2_2_DP	CLK_M2_2_DP 27
CLKOUT_PCIE_N10	P3	CLK_M2_2_DN	CLK_M2_2_DN 27
CLKOUT_PCIE_P11	T3		
CLKOUT_PCIE_N11	T2		
CLKOUT_PCIE_P12	U2		
CLKOUT_PCIE_N12	U1		
CLKOUT_PCIE_P13	AA5		
CLKOUT_PCIE_N13	Y7		
CLKOUT_PCIE_P14	R2		
CLKOUT_PCIE_N14	R3		
CLKOUT_PCIE_P15	T11		
CLKOUT_PCIE_N15	T13		

PCI_E2 — LAN
PCI_E4 — ASMEDIA1142
PCI_E1 — LAN
PCI_E3 — ASMEDIA1083
M.2
M.2

EMI
AZ_BITCLK — C576 X_10p50N4
AZ_SDOUT — C600 X_10p50N4

PCH1D

37 AZ_SDIN0	AZ_SDIN0		BA2	HDA_SDI0
			BB1	HDA_SDI1
18 AZ_SDOUT_R / 37 AZ_SDOUT	AZ_SDOUT_R / AZ_SDOUT	R657 33R/4 AZ_SDOUT_R	BC3	HDA_SDO
37 AZ_BITCLK	AZ_BITCLK	R640 33R/4 AZ_BITCLK_LR	BB3	HDA_BCLK
37 AZ_RST#	AZ_RST#	R642 33R/4 AZ_RST#_R	BC1	HDA_RST#
37 AZ_SYNC	AZ_SYNC	R676 33R/4 AZ_SYNC_R	BG6	HDA_SYNC

kb crb

AUDIO

4 PCH_CPU_AUD_SCLK	R574 30R/4	PCH_CPU_AUD_SCLK_R	AM2	DISPA_BCLK
4 PCH_CPU_AUD_SDO	R557 30R/4	PCH_CPU_AUD_SDO_R	AM3	DISPA_SDO
4 PCH_CPU_AUD_SDI		PCH_CPU_AUD_SDI	AN2	DISPA_SDI

AP36	AU43	GPP_D5 / I2S0_SFRM
AU43	AV44	GPP_D6 / I2S0_TXD
AV44	AU42	GPP_D7 / I2S0_RXD
AU42		GPP_D8 / I2S0_SCLK
AP42	AN43	GPP_D17 / DMIC_CLK1
AN43	AP38	GPP_D18 / DMIC_DATA1
AP38	AM43	GPP_D19 / DMIC_CLK0
AM43		GPP_D20 / DMIC_DATA0

PCH_H

PORT B

GPP_I5 / DDPB_CTRLCLK	AW5	HDMI_DDPB_CTRLCLK	HDMI_DDPB_CTRLCLK 36
GPP_I6 / DDPB_CTRLDATA	AV7	HDMI_DDPB_CTRLDATA	HDMI_DDPB_CTRLDATA 36
GPP_I0 / DDPB_HPD0	AP7	HDMI_DDPB_HPD	HDMI_DDPB_HPD 36

PORT C

GPP_I7 / DDPC_CTRLCLK	AT5	DVI_DDPC_CTRLCLK	DVI_DDPC_CTRLCLK 35
GPP_I8 / DDPC_CTRLDATA	BA6	DVI_DDPC_CTRLDATA	DVI_DDPC_CTRLDATA 35
GPP_I1 / DDPC_HPD1	AT8	DVI_DDPC_HPD	DVI_DDPC_HPD 35

PORT D

GPP_I9 / DDPD_CTRLCLK	AY1		
GPP_I10 / DDPD_CTRLDATA	AY2		
GPP_I2 / DDPD_HPD2	AP8	DDPE_HPD2	R615 10K/4

eDP

GPP_F19 / eDP_VDDEN	AC42		
GPP_F20 / eDP_BKLTEN	AE35		
GPP_F21 / eDP_BKLTCTL	AE36		
GPP_I4 / EDP_HPD	BA1	EDP_HPD	R641 100K/4
GPP_I3 / DDPE_HPD3	AT7	DDPE_HPD3	R600 10K/4

VCC3

HDMI_DDPB_CTRLCLK	R618	2.2K/4	
HDMI_DDPB_CTRLDATA	R620	2.2K/4	
DVI_DDPC_CTRLCLK	R619	2.2K/4	
DVI_DDPC_CTRLDATA	R621	2.2K/4	

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size	Document Description	Rev
Custom	PCH-USB/PCIE/DMI/SATA	10

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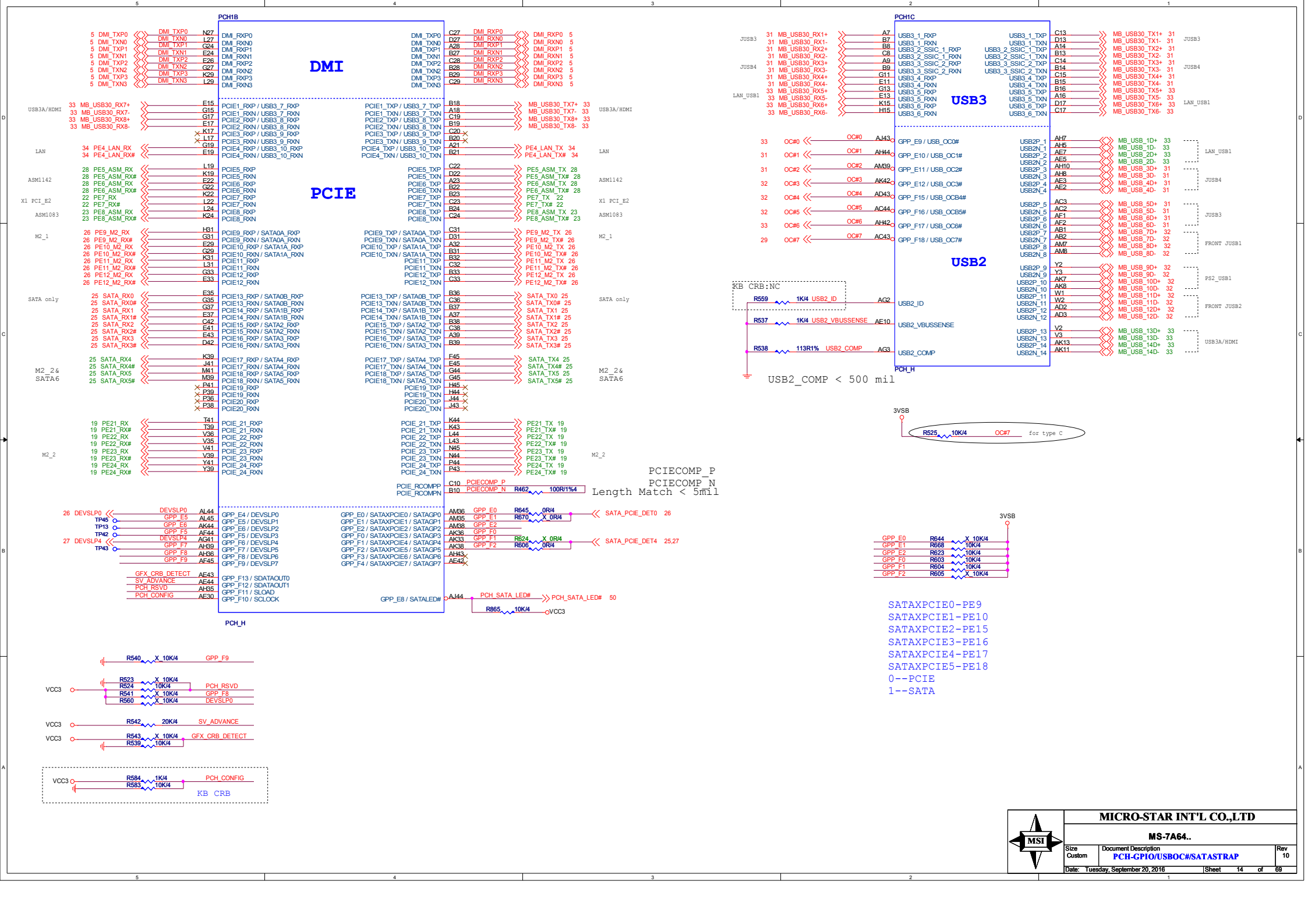
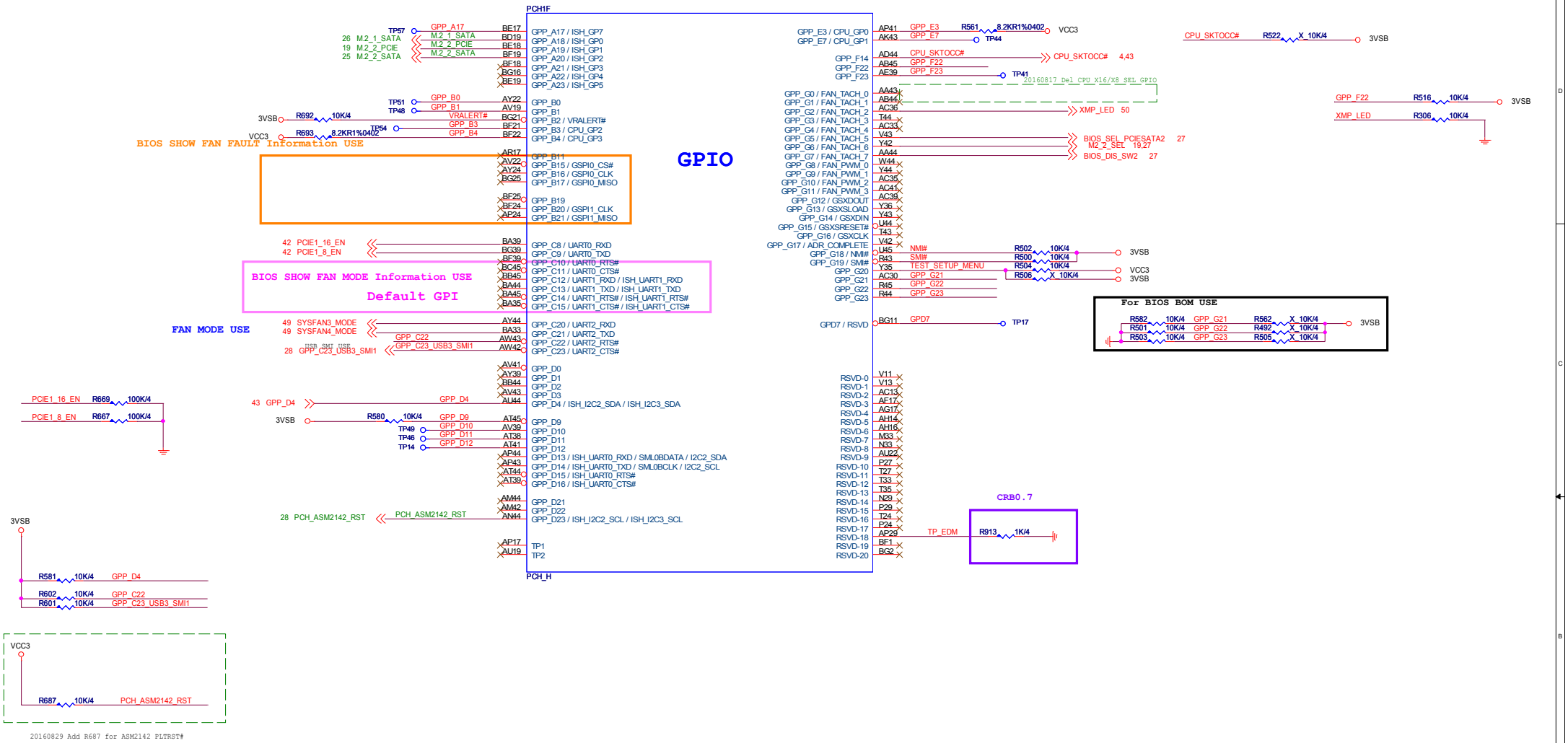


MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: PCH-GPIO/USBOC#/SATASTRAP
Rev: 10	
Date: Tuesday, September 20, 2016	Sheet 14 of 69



MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: PCH-LPC/SPI/SMBUS/MISC
Rev: 10	
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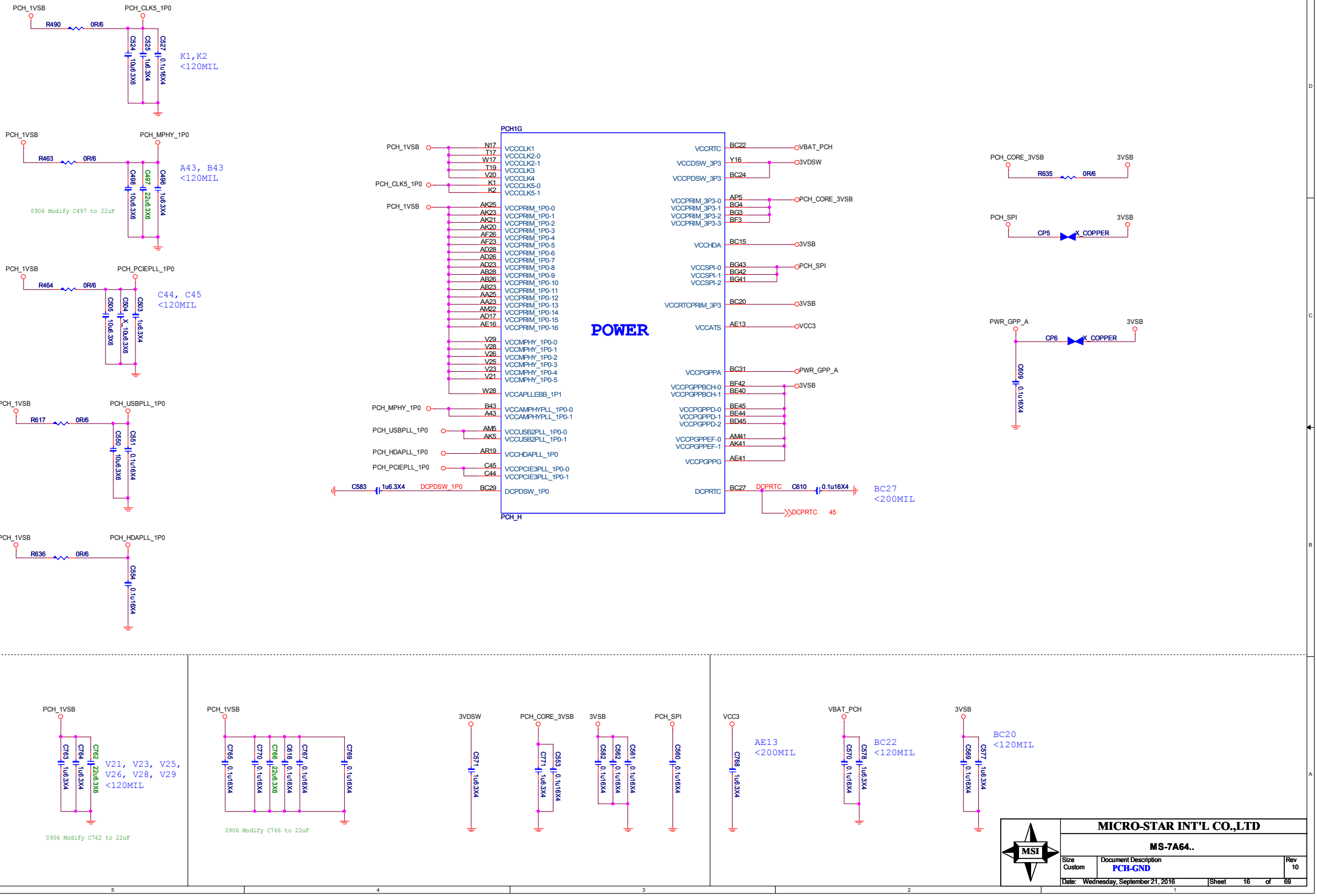
PCH_1VSB
PCH_CLK5_1P0
R490 0R/6
C524 10u6.3X6
C525 1u6.3X4
C527 0.1u16X4
K1,K2
<120MIL
PCH_1VSB
PCH_MPHY_1P0
R463 0R/6
C498 10u6.3X6
C497 22u6.3X6
C496 1u6.3X4
A43, B43
<120MIL
0906 Modify C497 to 22uF
PCH_1VSB
PCH_PCIEPLL_1P0
R464 0R/6
C505 10u6.3X6
C504 X 10u6.3X6
C503 1u6.3X4
C44, C45
<120MIL
PCH_1VSB
PCH_USBPLL_1P0
R617 0R/6
C550 10u6.3X6
C551 0.1u16X4
PCH_1VSB
PCH_HDAPLL_1P0
R636 0R/6
C554 0.1u16X4
PCH1G
POWER
PCH_H
PCH_1VSB
PCH_CLK5_1P0
PCH_1VSB
PCH_MPHY_1P0
PCH_USBPLL_1P0
PCH_HDAPLL_1P0
PCH_PCIEPLL_1P0
C583 1u6.3X4 DCPDSW_1P0
VCCCLK1
VCCCLK2-0
VCCCLK2-1
VCCCLK3
VCCCLK4
VCCCLK5-0
VCCCLK5-1
VCCPRIM_1P0-0
VCCPRIM_1P0-1
VCCPRIM_1P0-2
VCCPRIM_1P0-3
VCCPRIM_1P0-4
VCCPRIM_1P0-5
VCCPRIM_1P0-6
VCCPRIM_1P0-7
VCCPRIM_1P0-8
VCCPRIM_1P0-9
VCCPRIM_1P0-10
VCCPRIM_1P0-11
VCCPRIM_1P0-12
VCCPRIM_1P0-13
VCCPRIM_1P0-14
VCCPRIM_1P0-15
VCCPRIM_1P0-16
VCCMPHY_1P0-0
VCCMPHY_1P0-1
VCCMPHY_1P0-2
VCCMPHY_1P0-3
VCCMPHY_1P0-4
VCCMPHY_1P0-5
VCCAPLLEBB_1P1
VCCAMPHYPLL_1P0-0
VCCAMPHYPLL_1P0-1
VCCUSB2PLL_1P0-0
VCCUSB2PLL_1P0-1
VCCHDAPLL_1P0
VCCPCIE3PLL_1P0-0
VCCPCIE3PLL_1P0-1
DCPDSW_1P0
VCCRTC
VCCDSW_3P3
VCCPDSW_3P3
VCCPRIM_3P3-0
VCCPRIM_3P3-1
VCCPRIM_3P3-2
VCCPRIM_3P3-3
VCCHDA
VCCSPI-0
VCCSPI-1
VCCSPI-2
VCCRTCPRIM_3P3
VCCATS
VCCPGPPA
VCCPGPPBCH-0
VCCPGPPBCH-1
VCCPGPPD-0
VCCPGPPD-1
VCCPGPPD-2
VCCPGPPEF-0
VCCPGPPEF-1
VCCPGPPG
DCPRTC
BC22 VBAT_PCH
Y16 3VDSW
BC24
AP5 BG4 BG3 BF3 PCH_CORE_3VSB
BC15 3VSB
BG43 BG42 BG41 PCH_SPI
BC20 3VSB
AE13 VCC3
BC31 PWR_GPP_A
BF42 BE40 3VSB
BE45 BE44 BD45
AM41 AK41
AE41
BC27 DCPRTC C610 0.1u16X4
DCPRTC 45
BC27
<200MIL
PCH_CORE_3VSB
R635 0R/6
3VSB
PCH_SPI
CP5 X COPPER
3VSB
PWR_GPP_A
CP6 X COPPER
3VSB
C609 0.1u16X4
PCH_1VSB
C763 1u6.3X4
C764 1u6.3X4
C762 22u6.3X6
V21, V23, V25,
V26, V28, V29
<120MIL
0906 Modify C762 to 22uF
PCH_1VSB
C765 0.1u16X4
C770 0.1u16X4
C766 22u6.3X6
C618 0.1u16X4
C767 0.1u16X4
C769 0.1u16X4
0906 Modify C766 to 22uF
3VDSW
C571 1u6.3X4
PCH_CORE_3VSB
C771 1u6.3X4
C553 0.1u16X4
3VSB
C582 0.1u16X4
C562 0.1u16X4
C581 0.1u16X4
PCH_SPI
C560 0.1u16X4
VCC3
C768 1u6.3X4
AE13
<200MIL
VBAT_PCH
C570 0.1u16X4
C578 1u6.3X4
BC22
<120MIL
3VSB
C569 0.1u16X4
C577 1u6.3X4
BC20
<120MIL
MICRO-STAR INT'L CO.,LTD
MS-7A64..
Size Custom
Document Description PCH-GND
Rev 10
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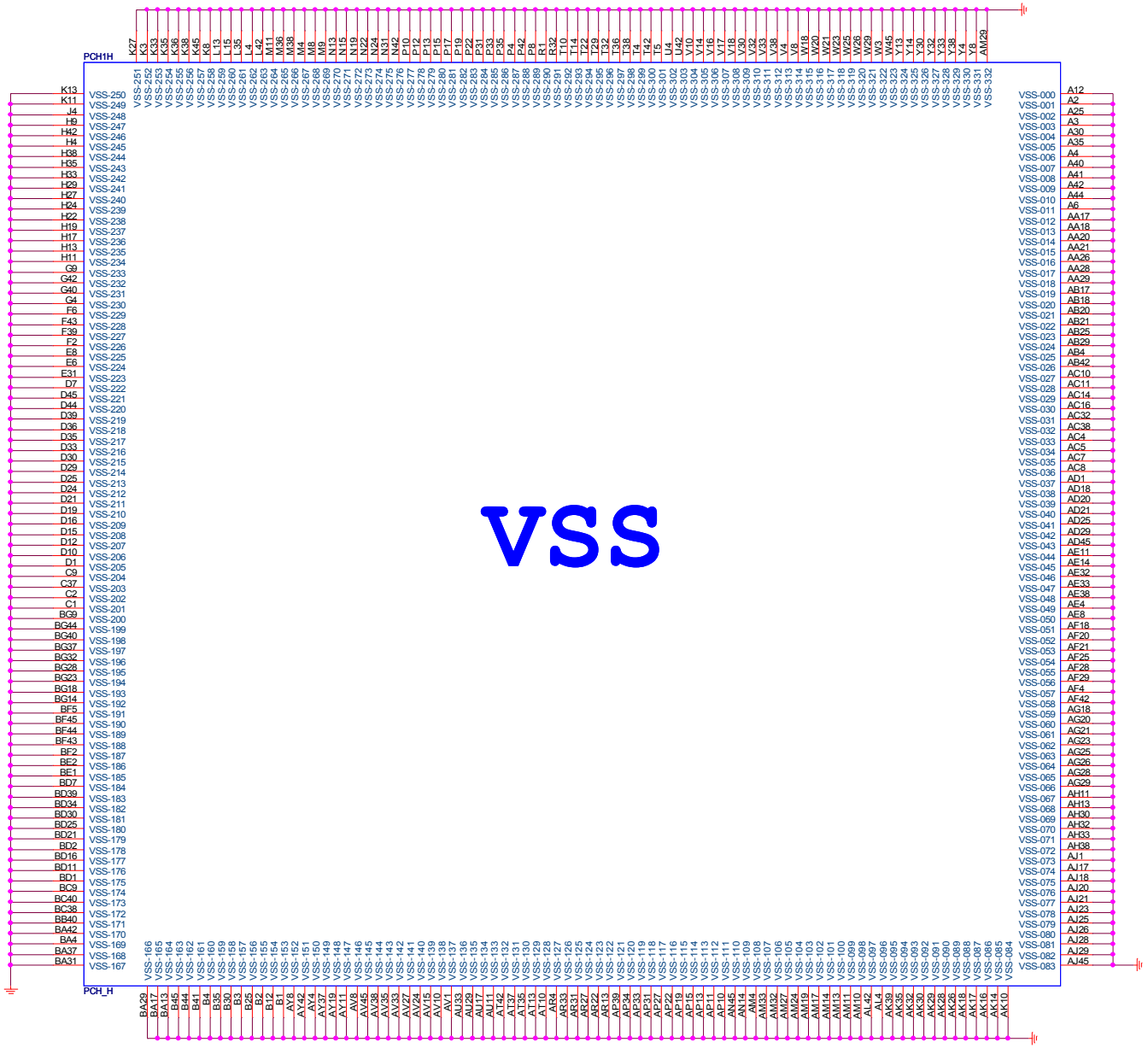

MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: PCH-Power	Rev: 10
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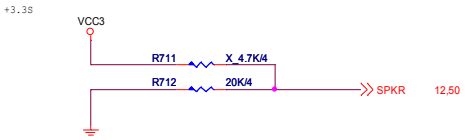
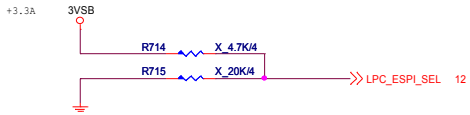
TOP Swap



Internal pull-down is disabled after PLTRST#

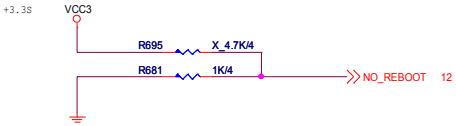
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

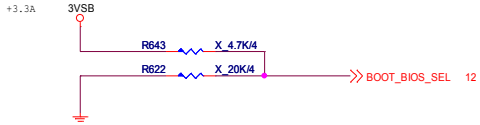
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

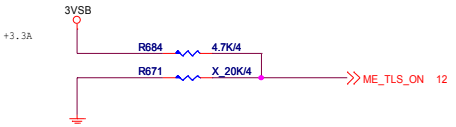
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

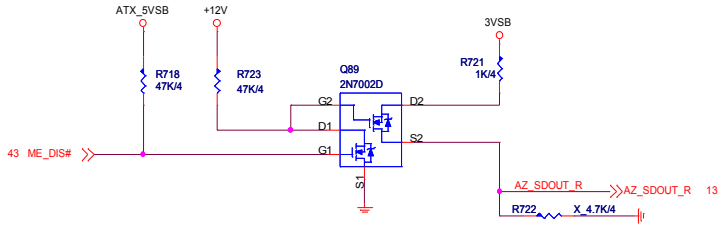
AMT and SBA with confidentiality



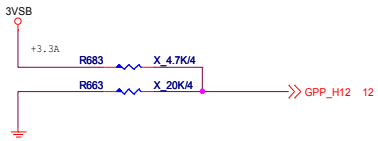
0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

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Size: Custom	Document Description: PCH-Strap	Rev: 10
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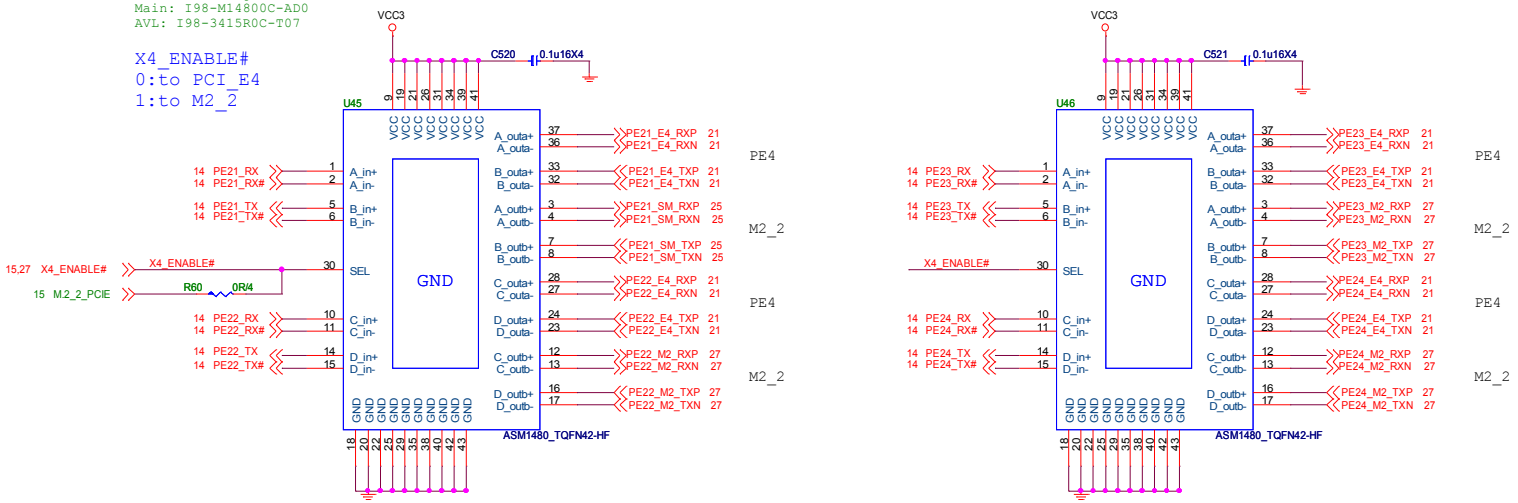
20160817 For PCI_E4 and M2_2 switch

20160804 Change Part
Main: I98-M14800C-AD0
AVL: I98-3415R0C-T07

X4_ENABLE#
0:to PCI_E4
1:to M2_2

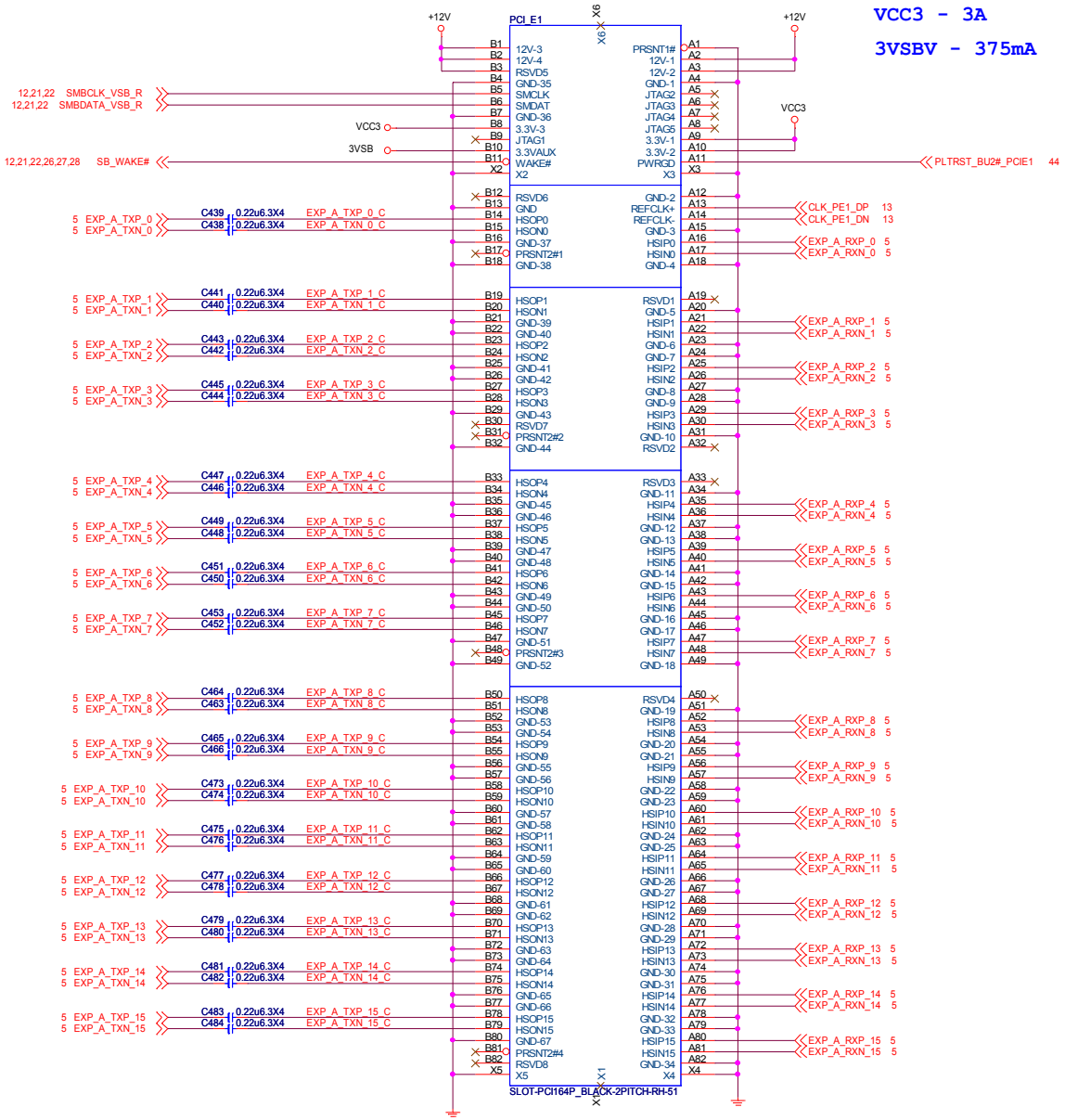


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
Size: Custom	Document Description: PCIE SWITCH	Rev: 10
Date: Wednesday, September 21, 2016	Sheet 19 of 69	

12V - 5.5A

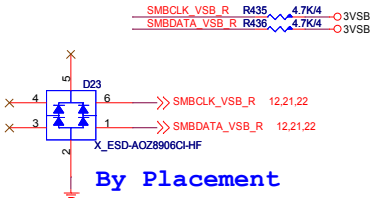
VCC3 - 3A

3VSBV - 375mA



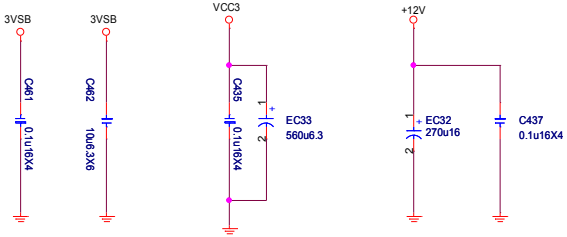
0906 Modify PCI_E1 PIN X2.X3.X4.X5 Connect to GND

SMBUS ESD



By Placement

Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

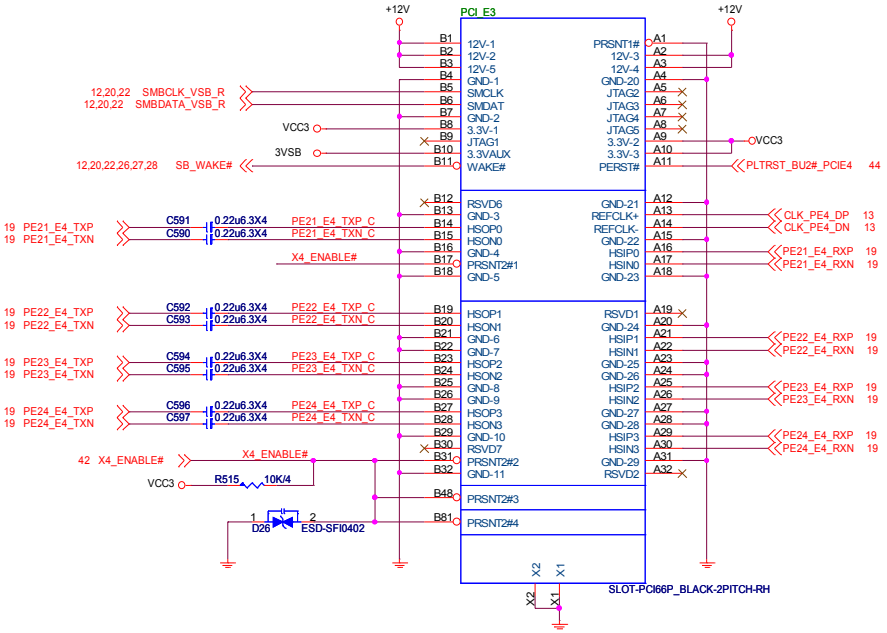


MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: PCIE SLOT (X16)
Rev: 10	
Date: Wednesday, September 21, 2016	Sheet 20 of 69

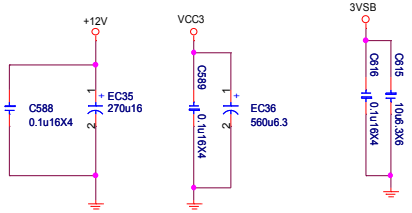
12V - 2.1A

VCC3 - 3A

3VSBV - 375mA



0909 Modify N11-1000221-L06 to N11-0660011-L06



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MS-7A64..

Size	Document Description	Rev
Custom	PCIE SLOT (X4)	10

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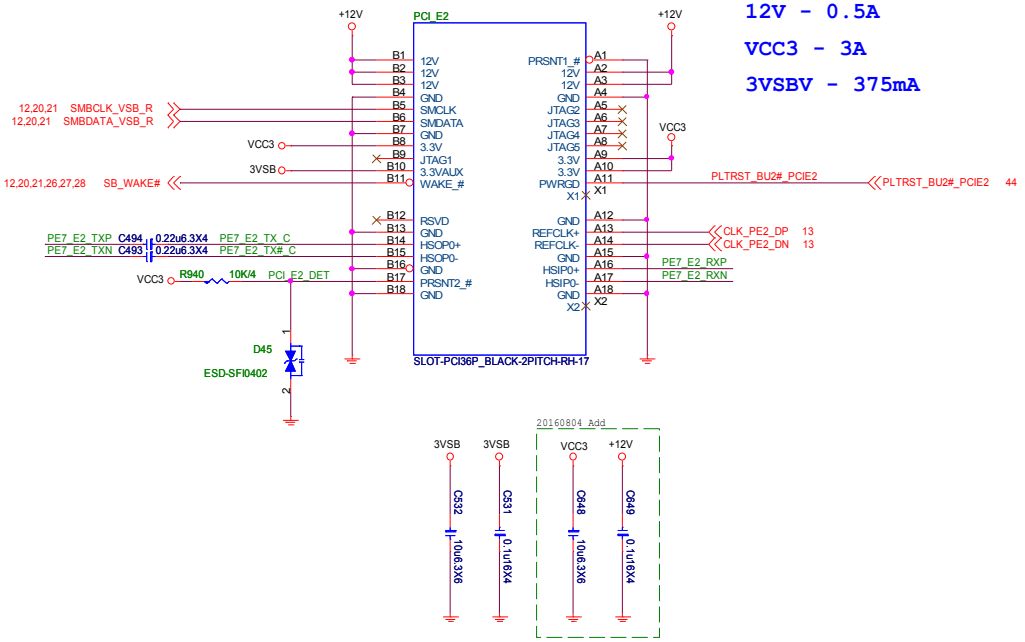

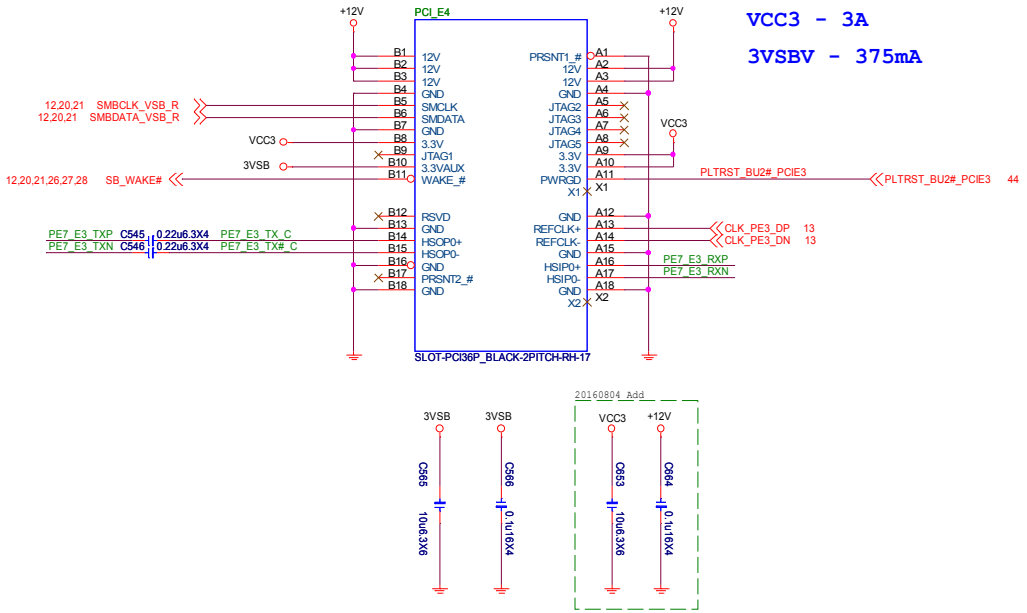

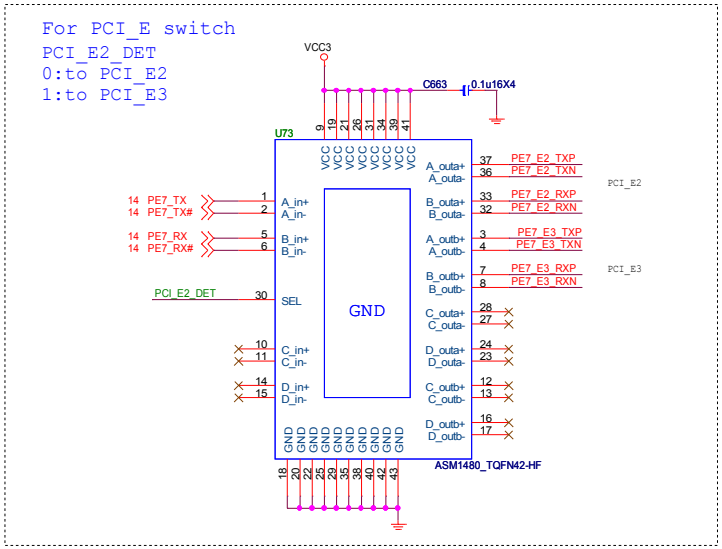

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MS-7A64..		
Size: Custom	Document Description: PCIE SLOT (X1)	Rev: 10
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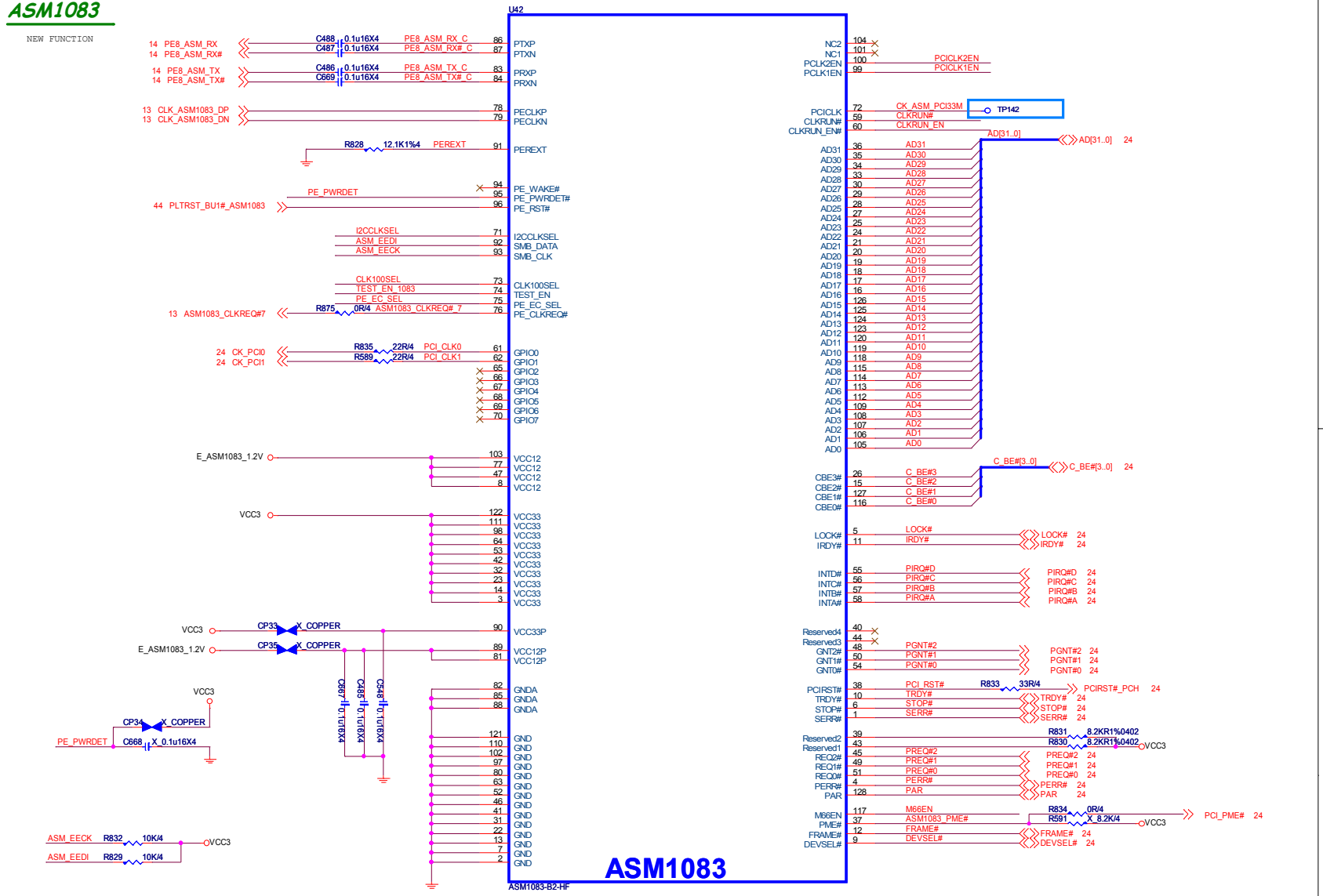
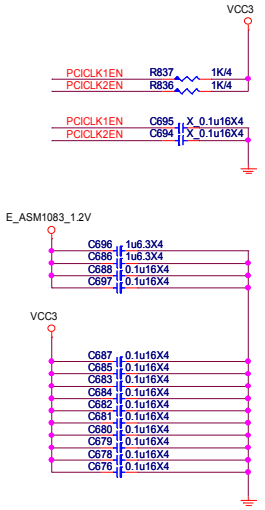
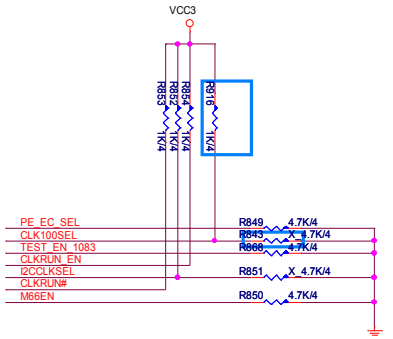
ASM1083

NEW FUNCTION





H/W Strapping



PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

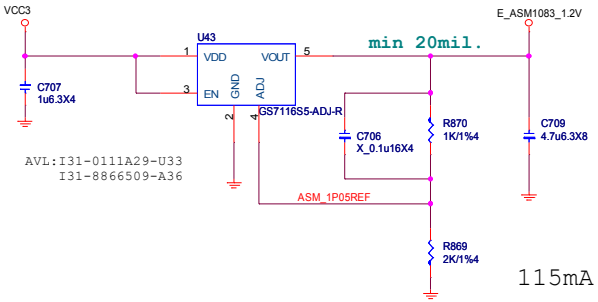
CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK

EMI

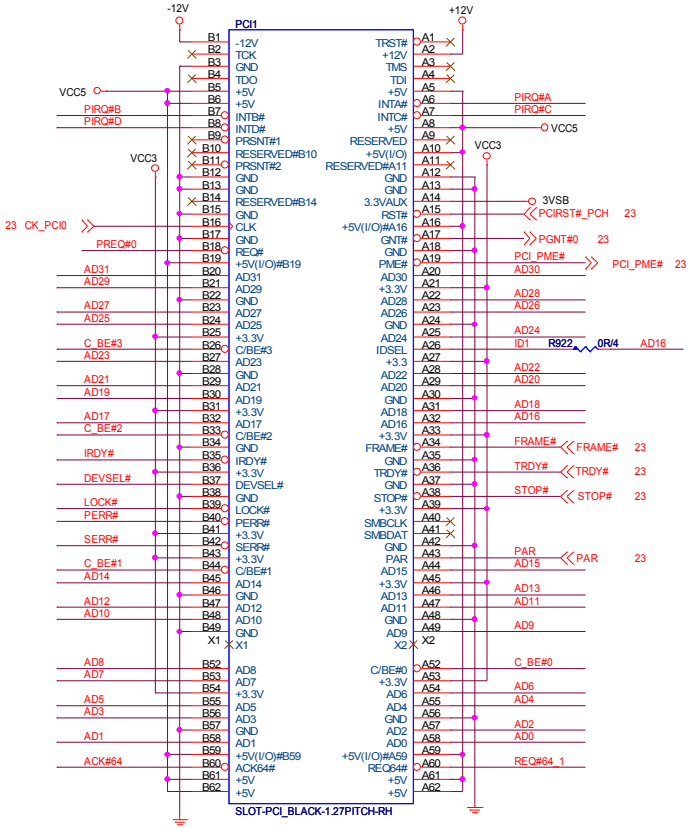
VCC3
90mA+115mA

Remove Cut Power.

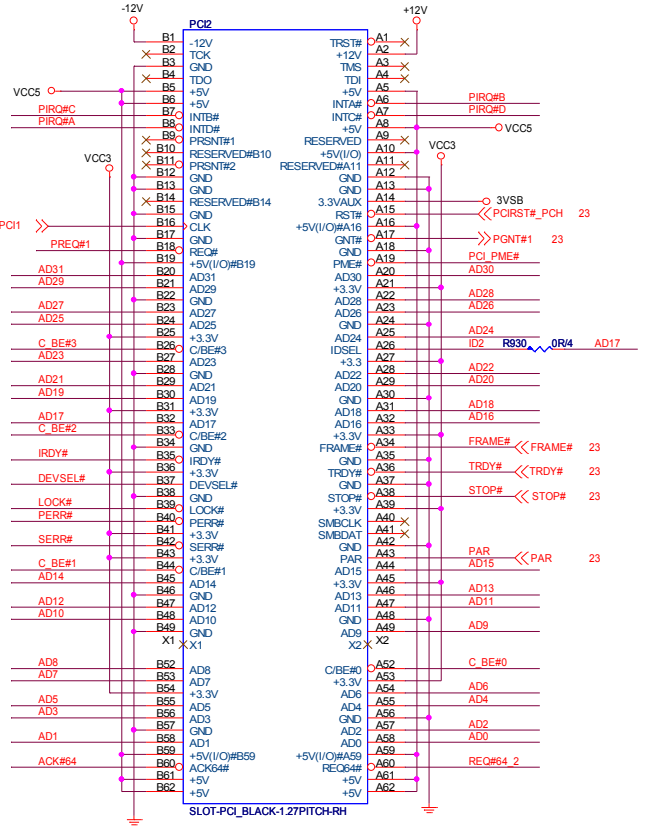


AVL:I31-0111A29-U33
I31-8866509-A36

MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: PCIE to PCI-ASM1083	Rev: 10
Date: Wednesday, September 21, 2016	Sheet 23 of 69	



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

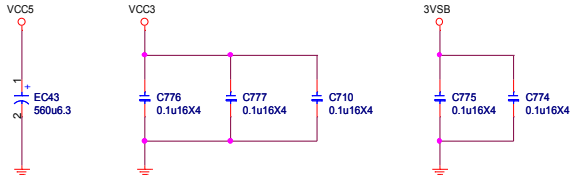


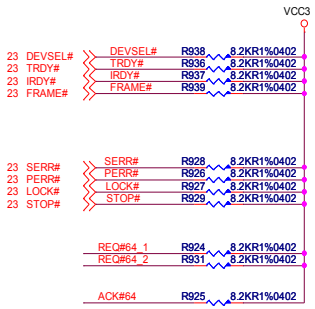
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

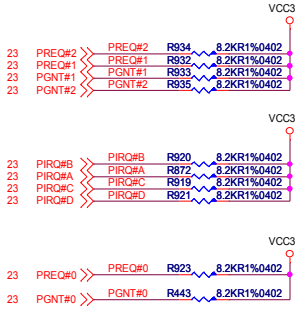
AD[31..0] AD[31..0] 23

C_BE#[3..0] C_BE#[3..0] 23

PCI PULL-UP / DOWN RESISTORS







PCI slot (X2)	
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 5A
+12V	- 500mA

MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size	Document Description	Rev
Custom	PCI SLOT	10

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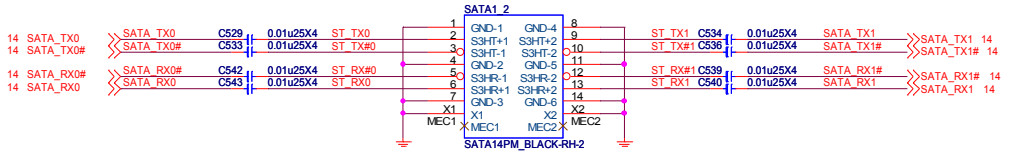

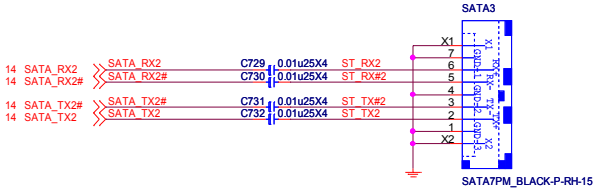

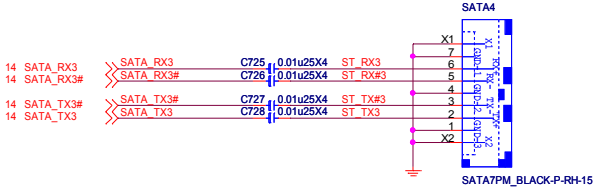

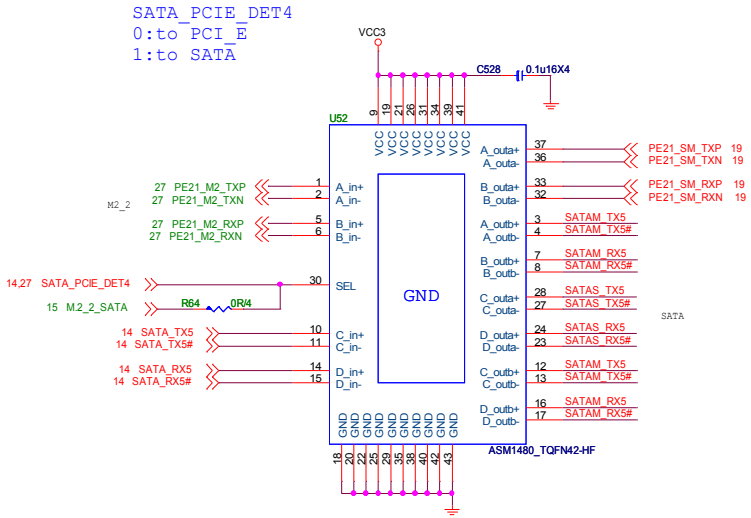

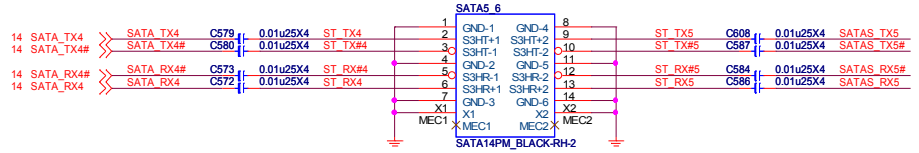

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MS-7A64..			
Size: Custom	Document Description: SATA Connector		Rev: 10
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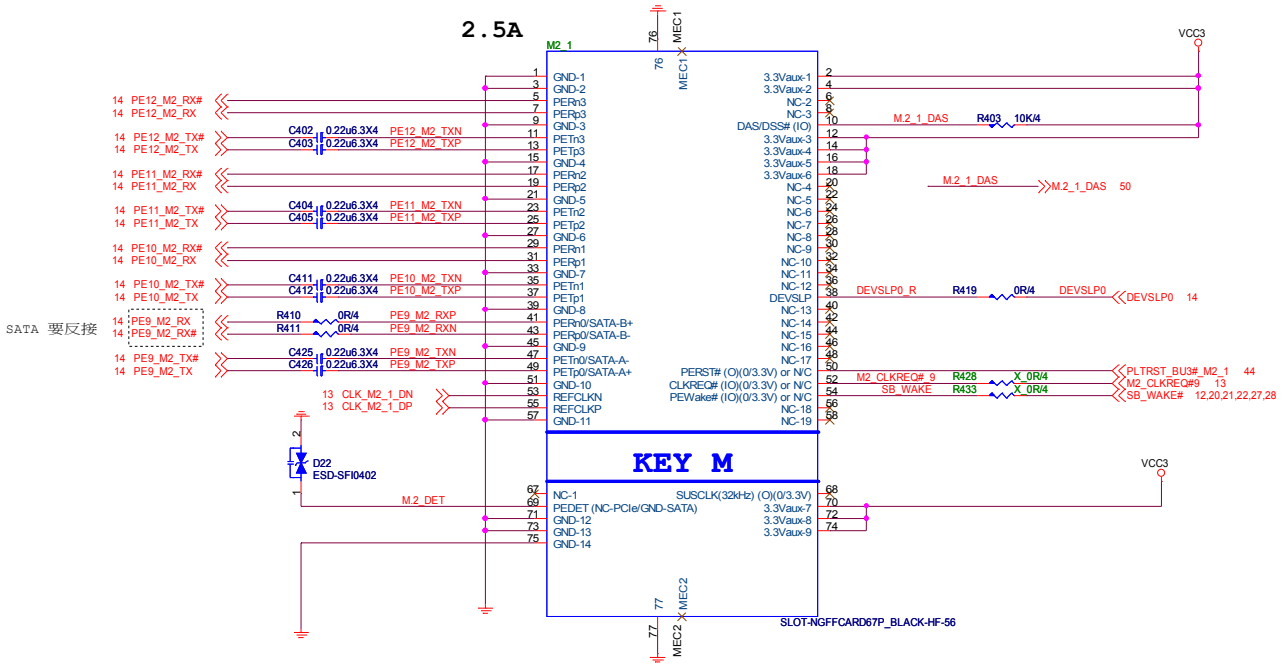
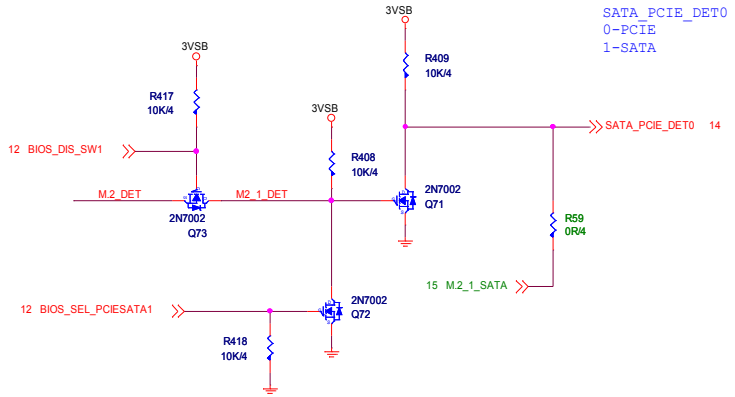
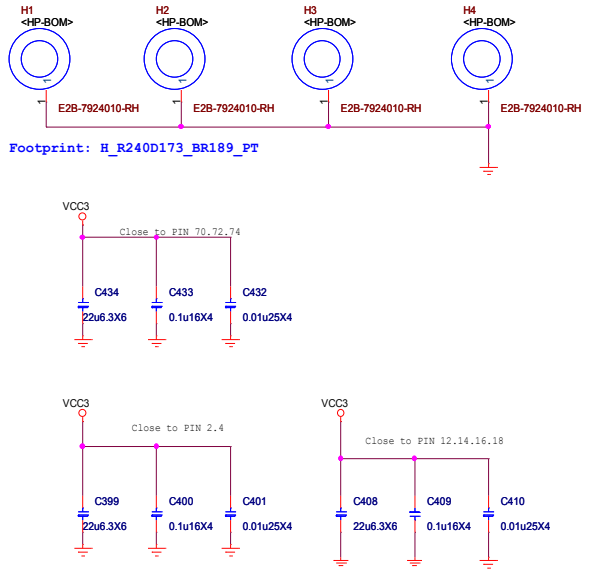




BIOS_MODE

GPP_H15	GPP_H13	
BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO



MICRO-STAR INT'L CO.,LTD

MS-7A64..

Size	Document Description	Rev
Custom	M.2-SLOT1	10

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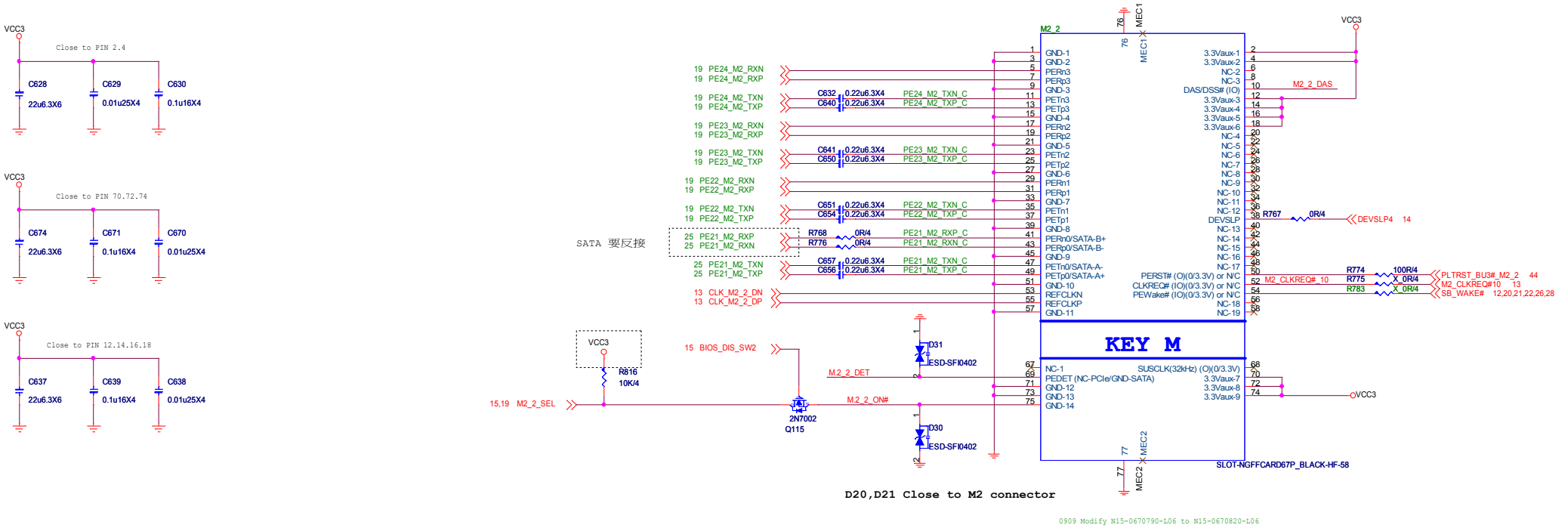

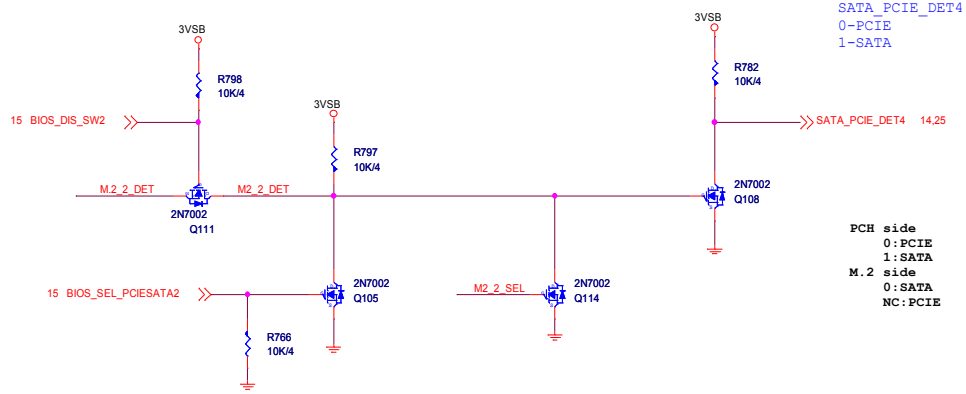

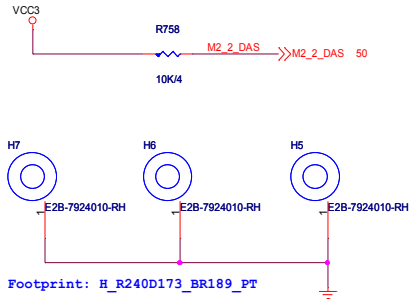

BIOS_MODE

GPP_G7	GPP_G6	GPP_G5	
BIOS_DIS_SW	***M2_2_SEL***	***BIOS_SEL_PCIESATA2***	***Mode***
GPI(1)	***GPI(1)***	***GPI(0)***	***AUTO***
0	*1*	*0*	***SATA6***
0	*0*	*1*	***M2-SATA***
0	*0*	*0*	***M2-PCIE***

MICRO-STAR INT'L CO.,LTD

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Power Consumption

	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	250mA	650mA	56mA	15mA	NA	1573.8(mW)
ASM2142	4mA	470mA	9mA	10mA	220mA	TDP

Minimun gap should be greater of >15mil with other signal.

USB HS (90Ohm-Diff) Chip to Connector ~1.5 inch.

USB SS (80Ohm-Diff)

USB HS (90Ohm-Diff)

USB SS (80Ohm-Diff)

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

PPON_X Internal Pull-up to VCC3

OCI_X Internal Pull-up to SUS

RX/TX Internal Pull-up

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

0909 Modify B02-021420C-AD0 to B02-021421C-AD0

Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

ASM1142 RU16 stuff RU17 unstuff
ASM2142 RU16 unstuff RU17 stuff

2016 . 8 .25 modification

ASM2142 U144 stuff RU24 unstuff
ASM1142 U144 unstuff RU24 stuff

YU1
D04-0900900-SC6(M)
D04-0901200-F07
D04-0901100-T16

X0/XI (95hm-Diff,Spacing 30mil)
UREXT,PEUREXT(W/S) : 10/7
OCIA,OCIB,PPONA,PPONB(W/S) : 5/8

ASM1142 RU19 stuff RU18 unstuff
ASM2142 RU19 unstuff RU18 stuff

atx5vsb change to vcc5

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

ASM1142 1.2 VCC Power

SN:L01-0107118-M26

20160829 Update

ASM1142 RU13/RU14 200K/187K 1.24V
ASM2142 RU13/RU14 196K/261K 1.05V

20160728
Change ASM1142 VDD/VDD_SUS to 1.24V from 1.2V base on data sheet R1.6 note1.

ASM1142 1.2 VSB Power

ASM1142 RU9 19.6K 1.2V
ASM2142 RU9 31.6K 1.05V

20160720
Add SPI ROM PN
1M bit for ASM2142
512K bit for ASM1142

EEPROM

ASM1142 UU3 M31-2551222-M24(512K bit)
ASM2142 UU3 M31-2511022-M24(1M bit)

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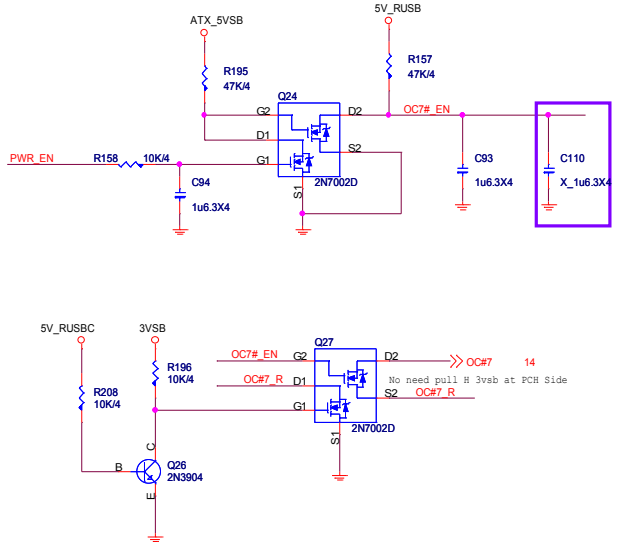
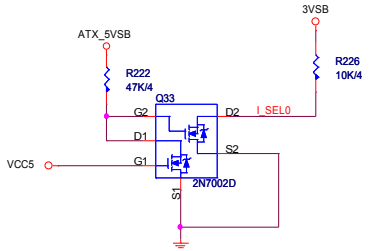
VBUS OC#



Current Mode

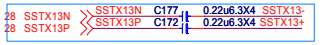


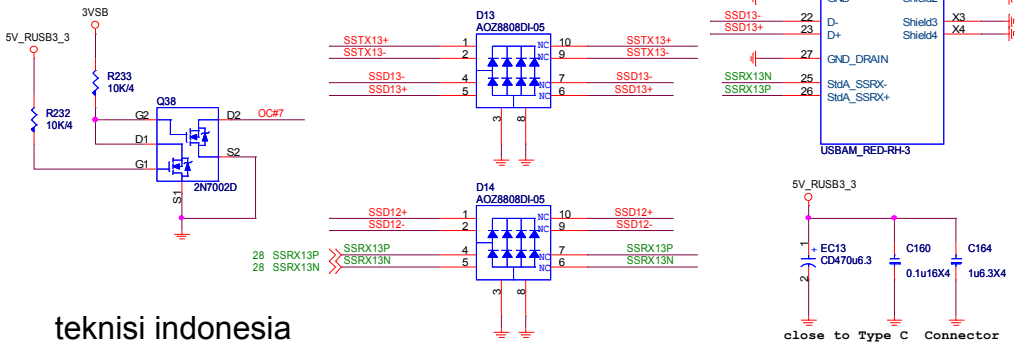
I_SEL0 : I_SEL1

X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

TYPE-A





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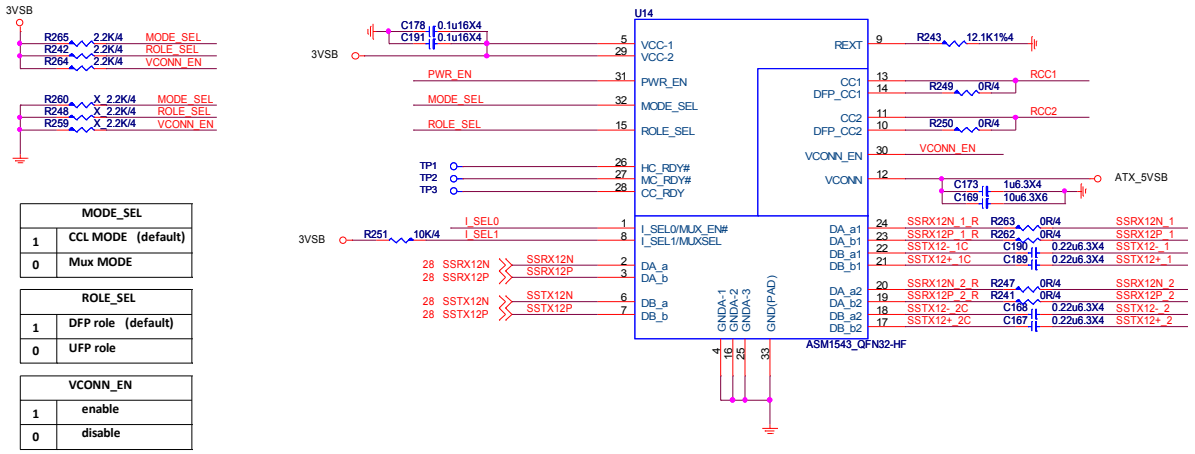
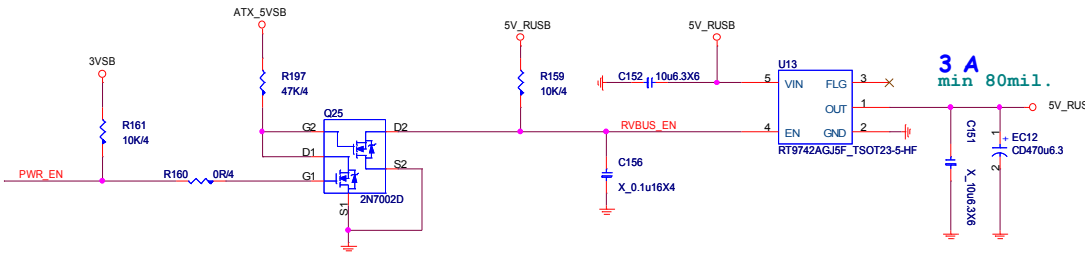
USB Type-C MUX with Configuration Channel (CC)



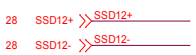
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

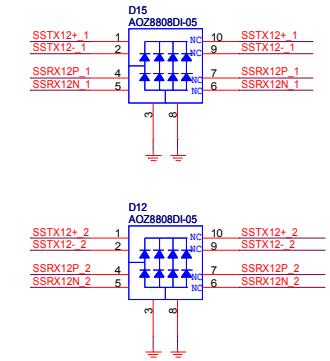
ROLE_SEL	
1	DFP role (default)
0	UFP role

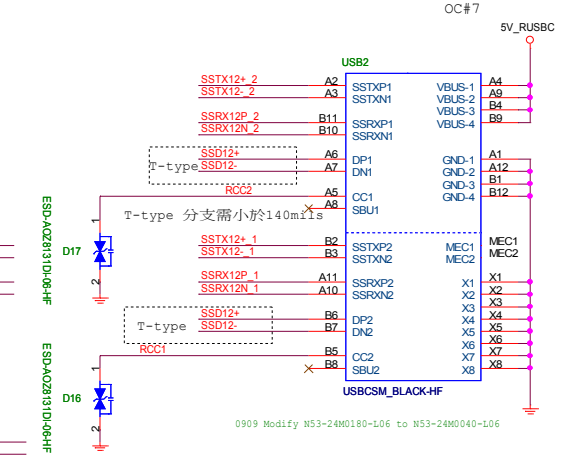
VCONN_EN	
1	enable
0	disable



TYPE-C

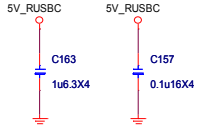






USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-005 AVL

close to Type C Connector



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Size: Custom	Document Description: USB TYPE C		Rev: 10
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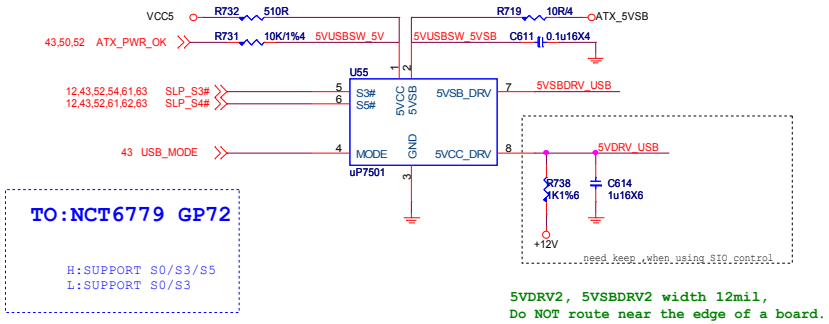
USB PORT POWER

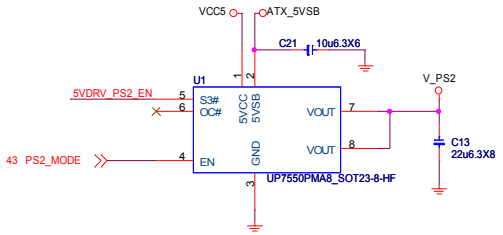


TO:NCT6779 GP72

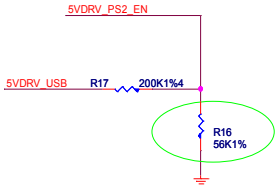
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3

5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

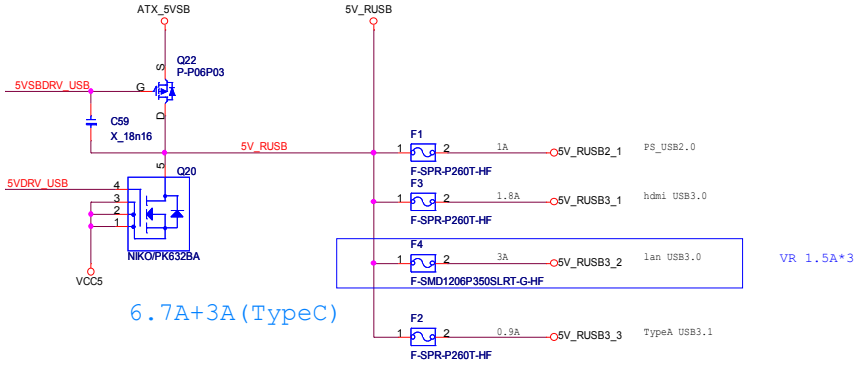
PS2 Power



USB MODE



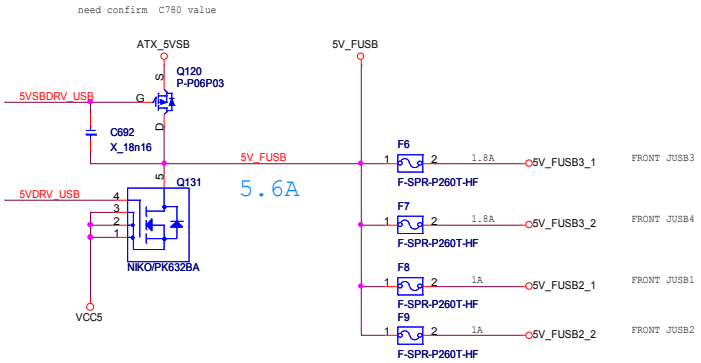
REAR USB PORT POWER



VR 1.5A*3

6.7A+3A(TypeC)

FRONT USB PORT POWER



5.6A

D08-0301000-P16
D08-0301100-B07

P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

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Size: Custom	Document Description: USB POWER UP7501	Rev: 10
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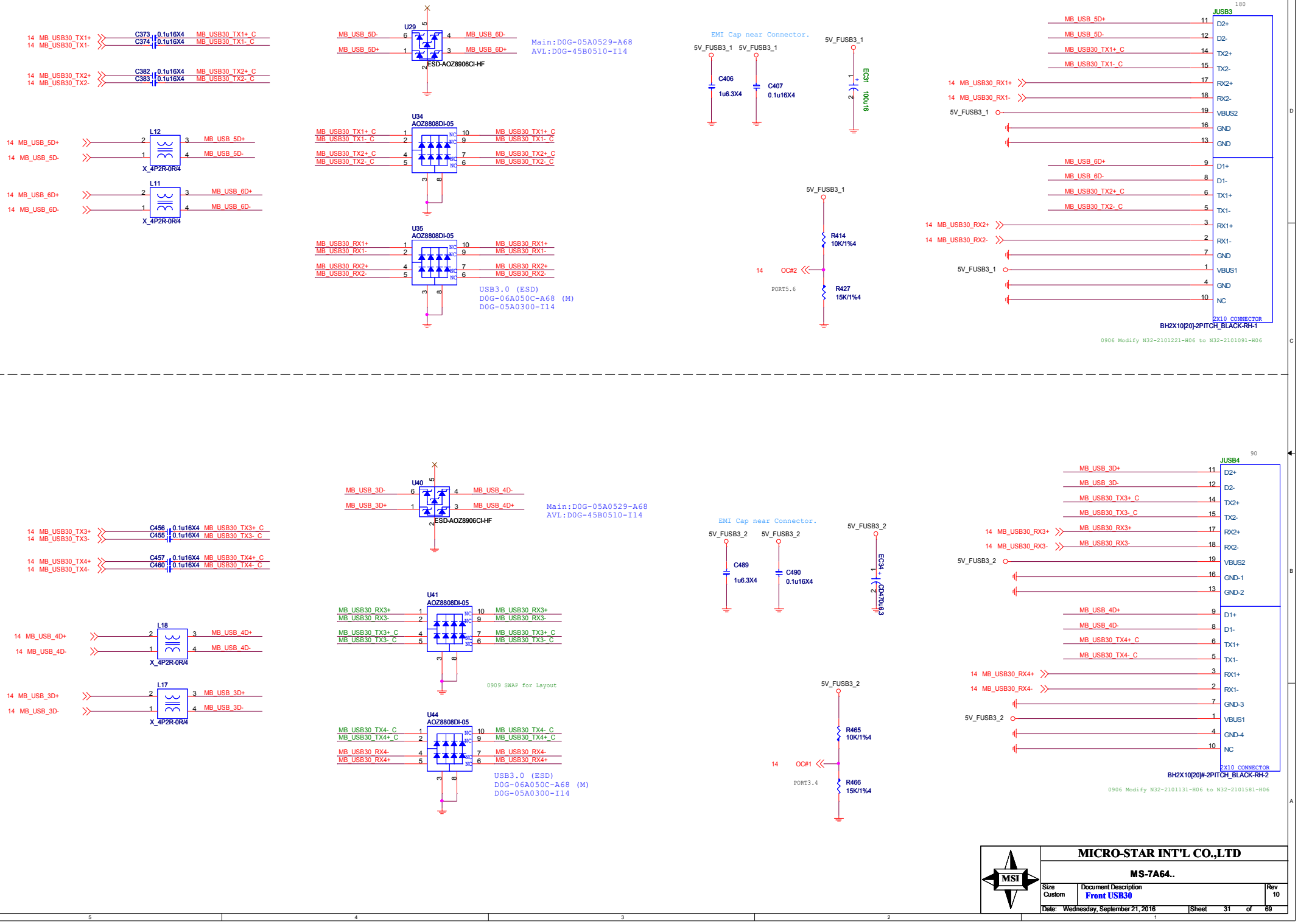
14 MB_USB30_TX1+
14 MB_USB30_TX1-
C373 0.1u16X4
C374 0.1u16X4
MB_USB30_TX1+_C
MB_USB30_TX1-_C
14 MB_USB30_TX2+
14 MB_USB30_TX2-
C382 0.1u16X4
C383 0.1u16X4
MB_USB30_TX2+_C
MB_USB30_TX2-_C
L12
14 MB_USB_5D+
14 MB_USB_5D-
MB_USB_5D+
MB_USB_5D-
X_4P2R-0R/4
L11
14 MB_USB_6D+
14 MB_USB_6D-
MB_USB_6D+
MB_USB_6D-
X_4P2R-0R/4
U29
MB_USB_5D-
MB_USB_5D+
MB_USB_6D-
MB_USB_6D+
ESD-AOZ8906CI-HF
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14
U34
AOZ8808DI-05
MB_USB30_TX1+_C
MB_USB30_TX1-_C
MB_USB30_TX2+_C
MB_USB30_TX2-_C
U35
AOZ8808DI-05
MB_USB30_RX1+
MB_USB30_RX1-
MB_USB30_RX2+
MB_USB30_RX2-
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
EMI Cap near Connector.
5V_FUSB3_1
C406 1u6.3X4
C407 0.1u16X4
EC31 100u16
R414 10K/1%4
14 OC#2
PORT5.6
R427 15K/1%4
JUSB3
MB_USB_5D+
MB_USB_5D-
MB_USB30_TX1+_C
MB_USB30_TX1-_C
14 MB_USB30_RX1+
14 MB_USB30_RX1-
5V_FUSB3_1
GND
VBUS2
MB_USB_6D+
MB_USB_6D-
MB_USB30_TX2+_C
MB_USB30_TX2-_C
14 MB_USB30_RX2+
14 MB_USB30_RX2-
VBUS1
NC
2X10 CONNECTOR
BH2X10[20]-2PITCH_BLACK-RH-1
0906 Modify N32-2101221-H06 to N32-2101091-H06
14 MB_USB30_TX3+
14 MB_USB30_TX3-
C456 0.1u16X4
C455 0.1u16X4
MB_USB30_TX3+_C
MB_USB30_TX3-_C
14 MB_USB30_TX4+
14 MB_USB30_TX4-
C457 0.1u16X4
C460 0.1u16X4
MB_USB30_TX4+_C
MB_USB30_TX4-_C
L18
14 MB_USB_4D+
14 MB_USB_4D-
MB_USB_4D+
MB_USB_4D-
X_4P2R-0R/4
L17
14 MB_USB_3D+
14 MB_USB_3D-
MB_USB_3D+
MB_USB_3D-
X_4P2R-0R/4
U40
MB_USB_3D-
MB_USB_3D+
MB_USB_4D-
MB_USB_4D+
ESD-AOZ8906CI-HF
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14
U41
AOZ8808DI-05
MB_USB30_RX3+
MB_USB30_RX3-
MB_USB30_TX3+_C
MB_USB30_TX3-_C
0909 SWAP for Layout
U44
AOZ8808DI-05
MB_USB30_TX4-_C
MB_USB30_TX4+_C
MB_USB30_RX4-
MB_USB30_RX4+
USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14
EMI Cap near Connector.
5V_FUSB3_2
C489 1u6.3X4
C490 0.1u16X4
EC34 CD470u6.3
R465 10K/1%4
14 OC#1
PORT3.4
R466 15K/1%4
JUSB4
MB_USB_3D+
MB_USB_3D-
MB_USB30_TX3+_C
MB_USB30_TX3-_C
14 MB_USB30_RX3+
14 MB_USB30_RX3-
5V_FUSB3_2
GND-1
GND-2
MB_USB_4D+
MB_USB_4D-
MB_USB30_TX4+_C
MB_USB30_TX4-_C
14 MB_USB30_RX4+
14 MB_USB30_RX4-
GND-3
GND-4
BH2X10[20]#-2PITCH_BLACK-RH-2
0906 Modify N32-2101131-H06 to N32-2101581-H06
MICRO-STAR INT'L CO.,LTD
MS-7A64..
Size Custom
Document Description
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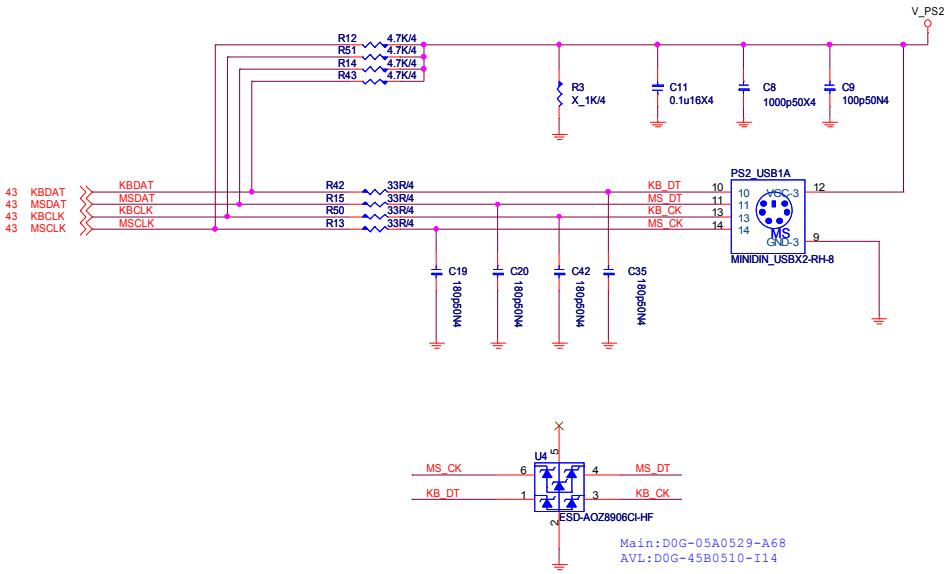
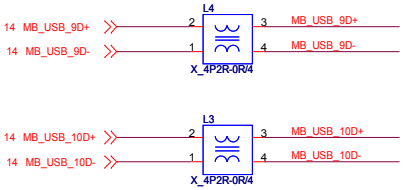
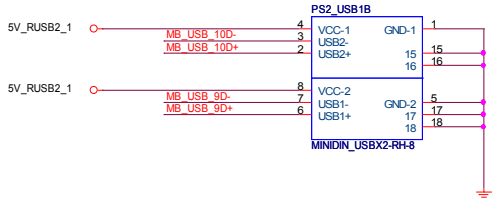
PS2 Connector

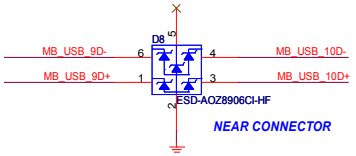


PS2 _USB

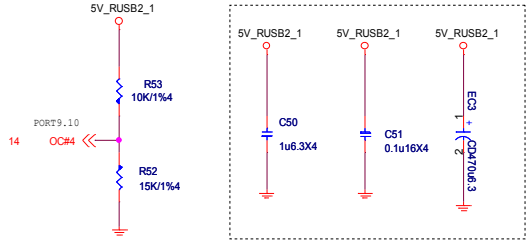


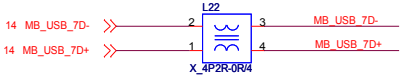


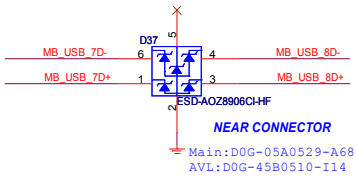
Main:D0G-05A0529-A68
AVL:D0G-45B0510-I14

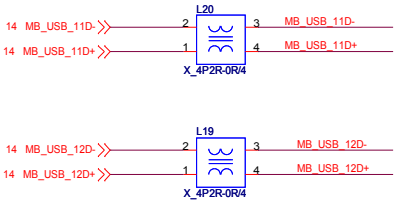


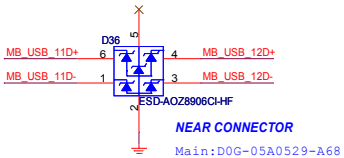
Close to Connector



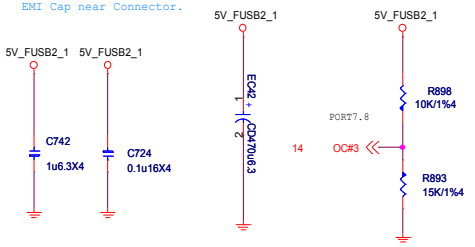




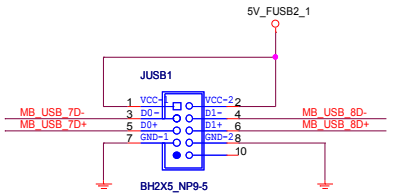




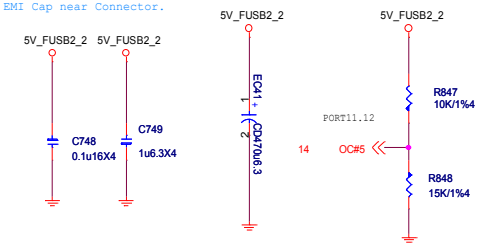
EMI Cap near Connector.



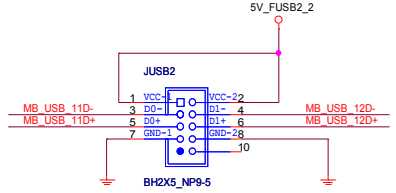
1.0A



EMI Cap near Connector.



1.0A



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MS-7A64..	
Size: Custom	Document Description: Real USB2&PS2 / Front USB2.0
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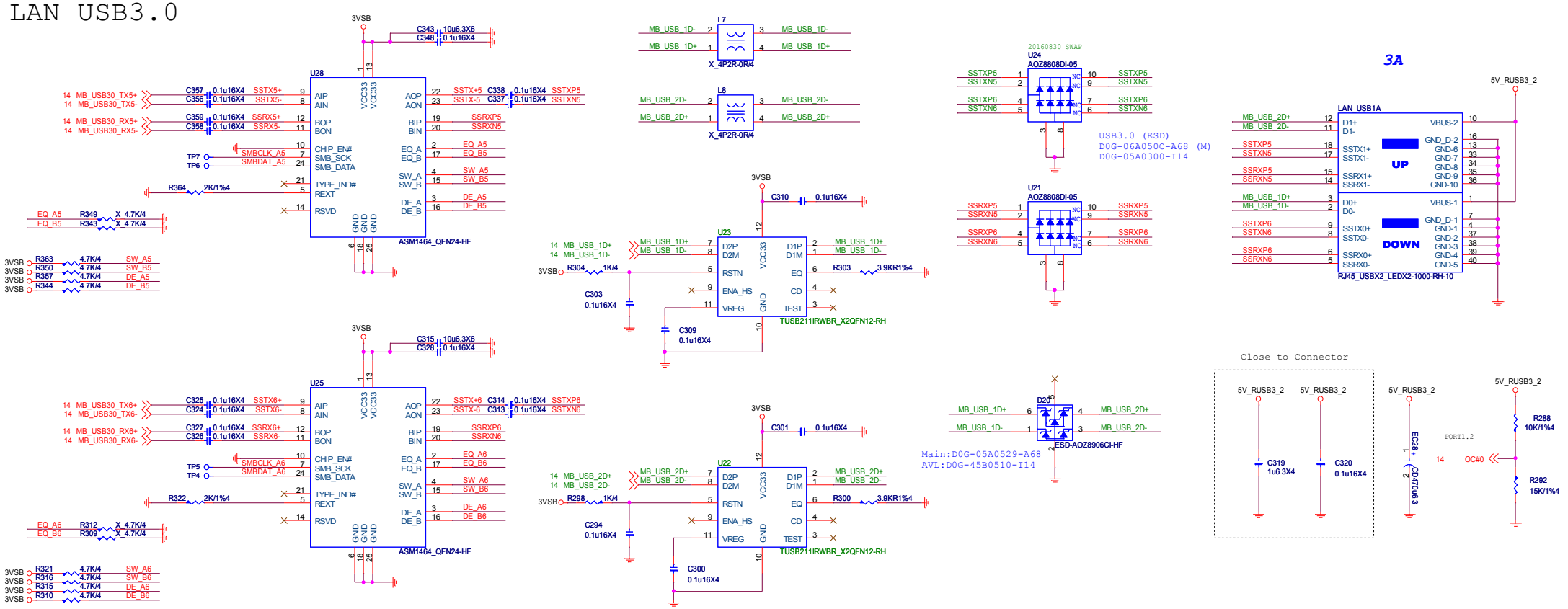
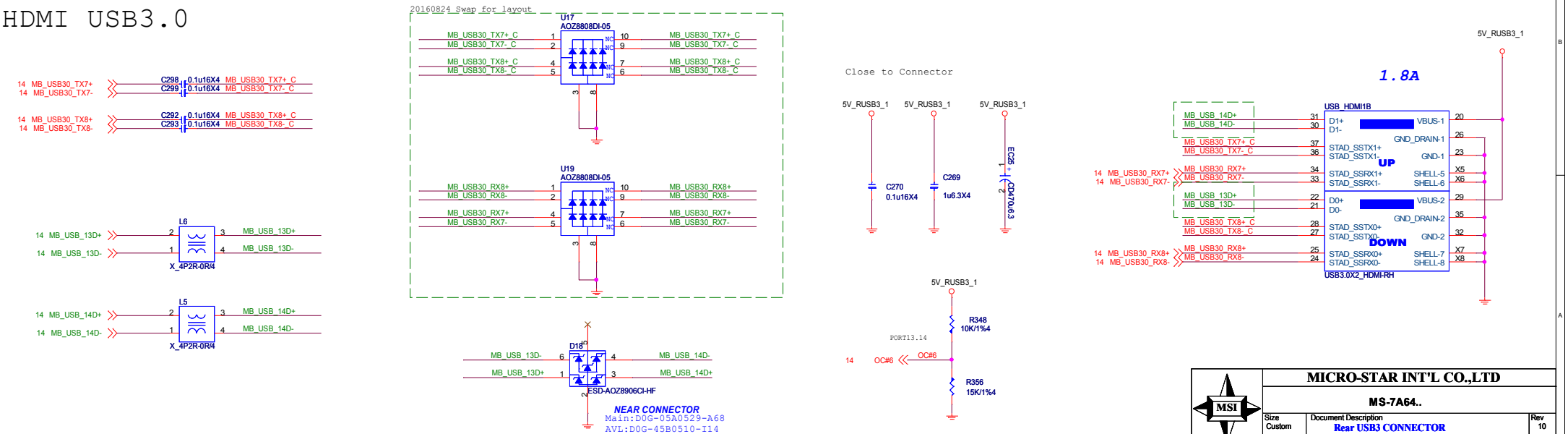
LAN USB3.0



HDMI USB3.0



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	MS-7A64..	
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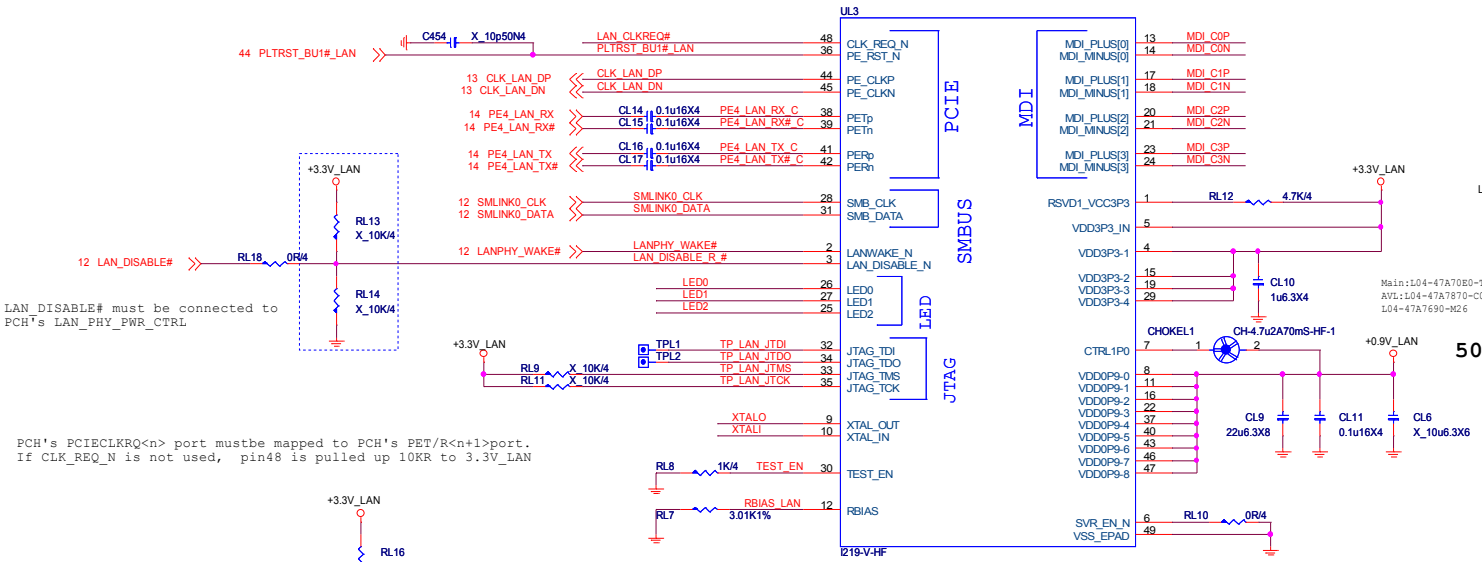
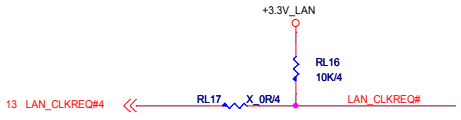
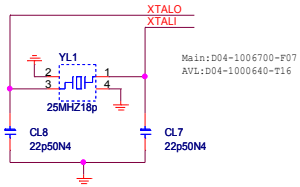
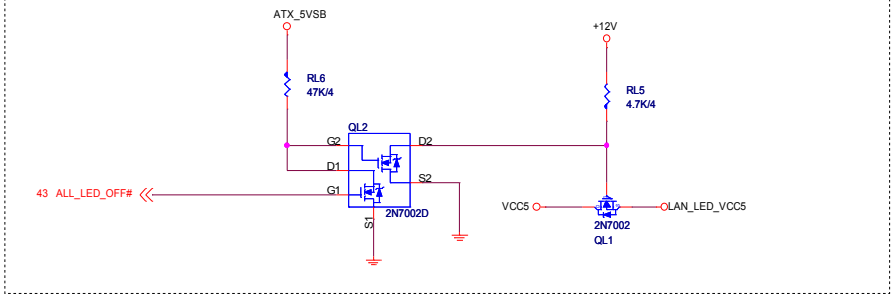
Intel Lan- i219

8111H:B06-08111CC-R09
8111G:B06-081116C-R09

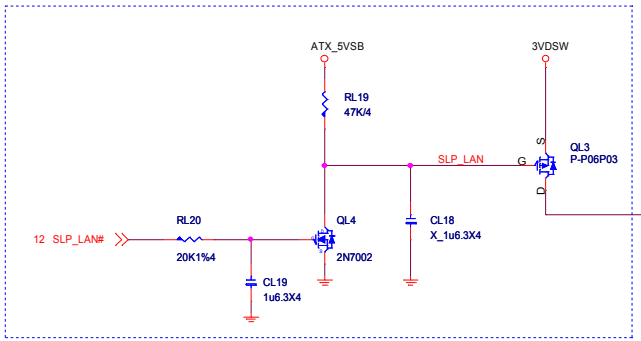


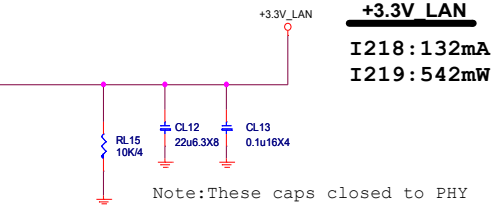






support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

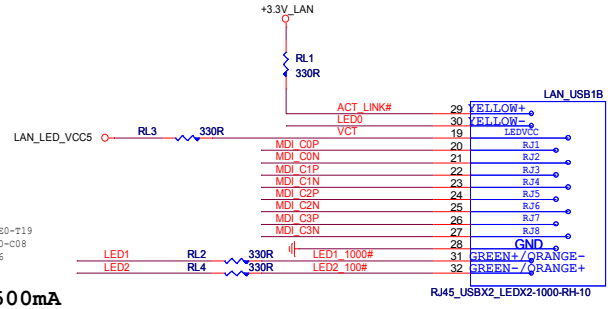




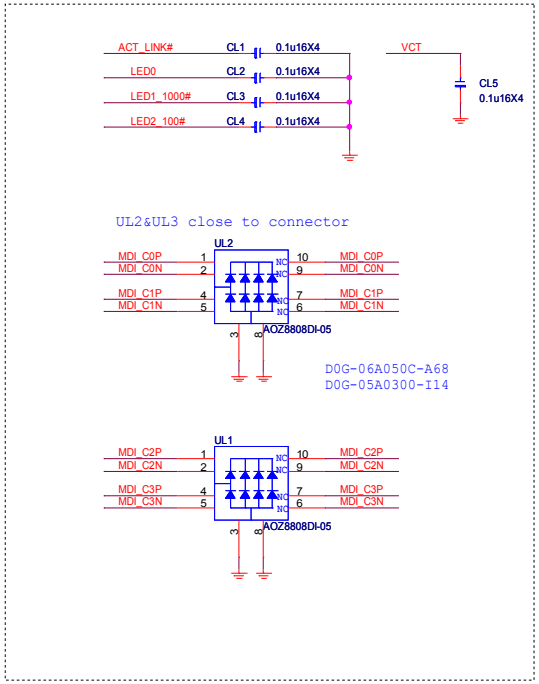
+3.3V_LAN

I218:132mA
I219:542mW

LAN Connector



For EMI



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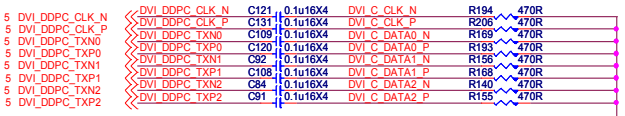
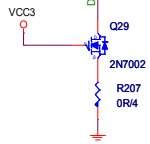
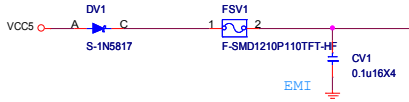
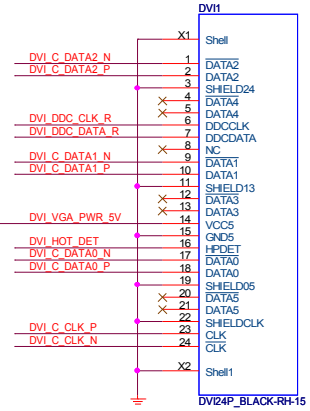
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)









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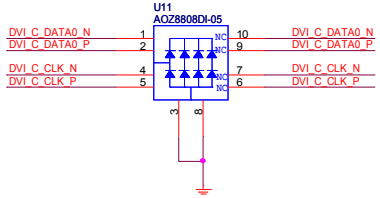
D0G-06A050C-A68



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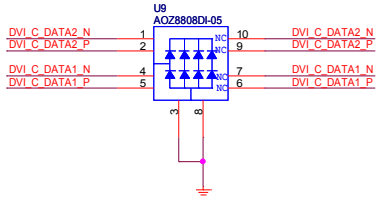
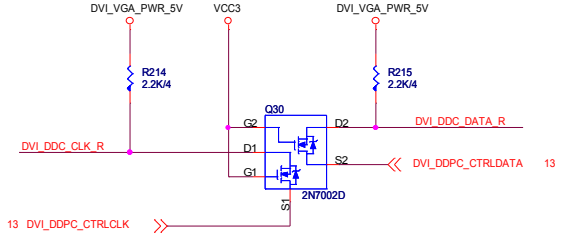
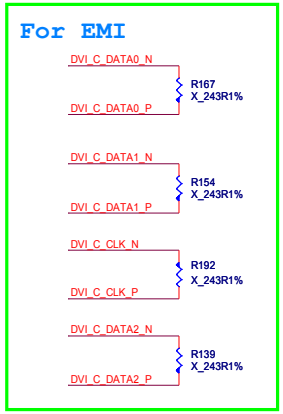
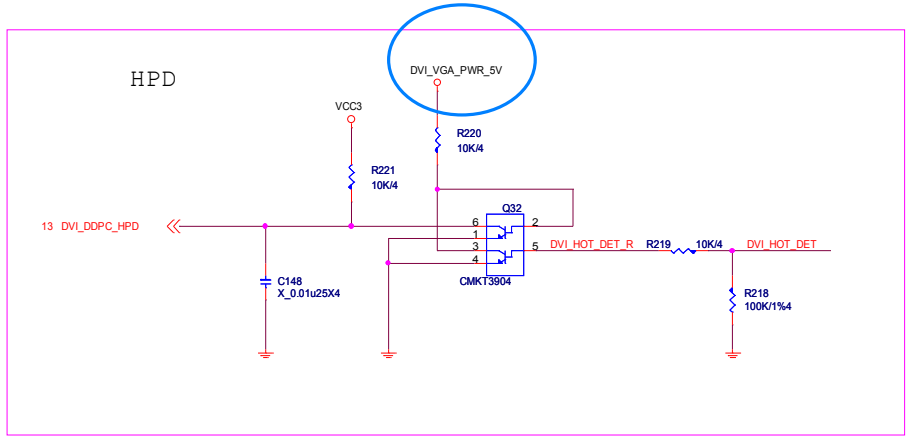
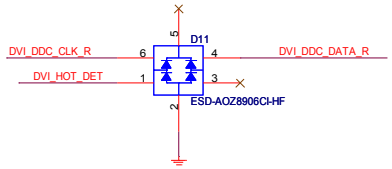
D0G-06A050C-A68











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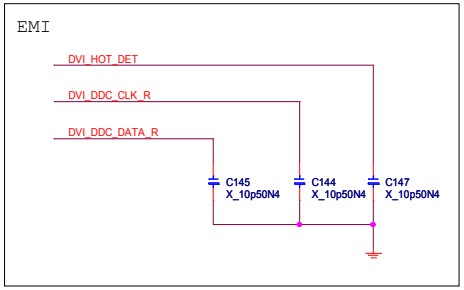

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HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

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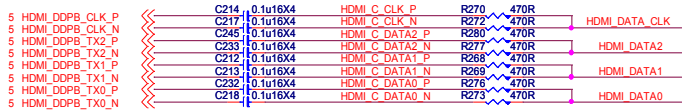

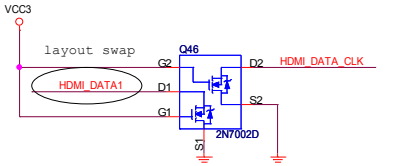

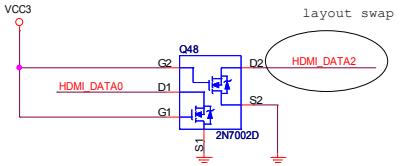

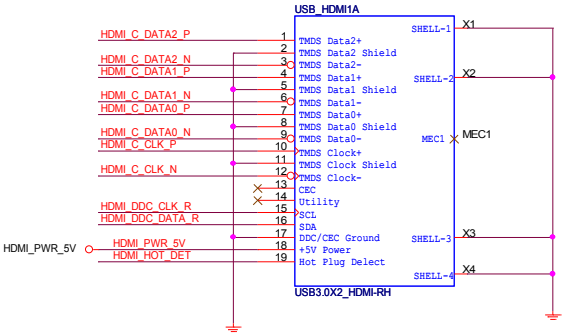

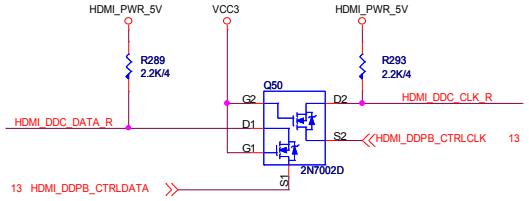

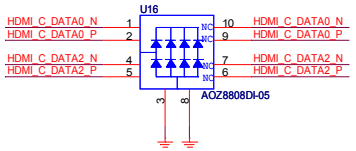

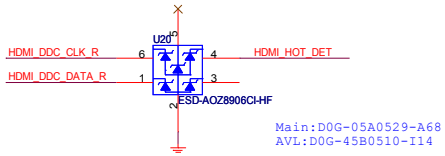

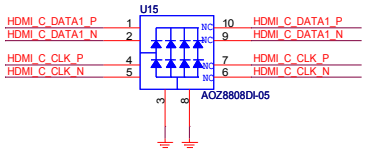

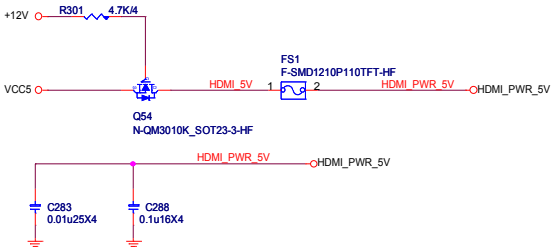

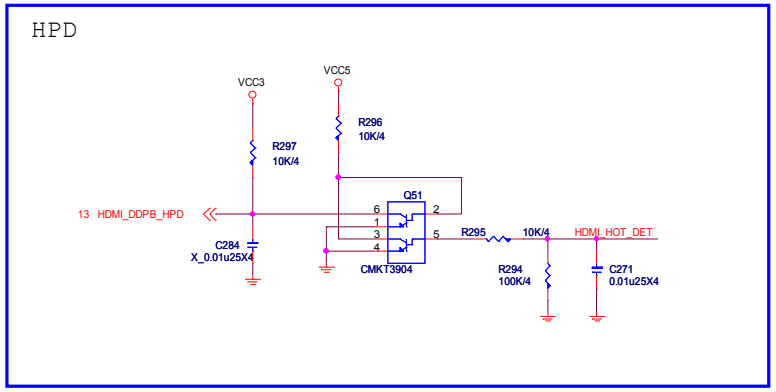

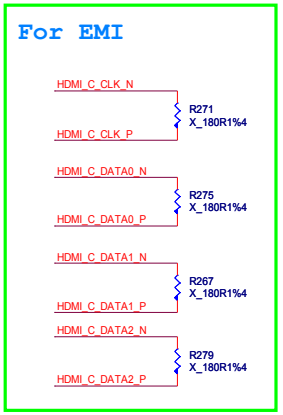

MICRO-STAR INT'L CO.,LTD

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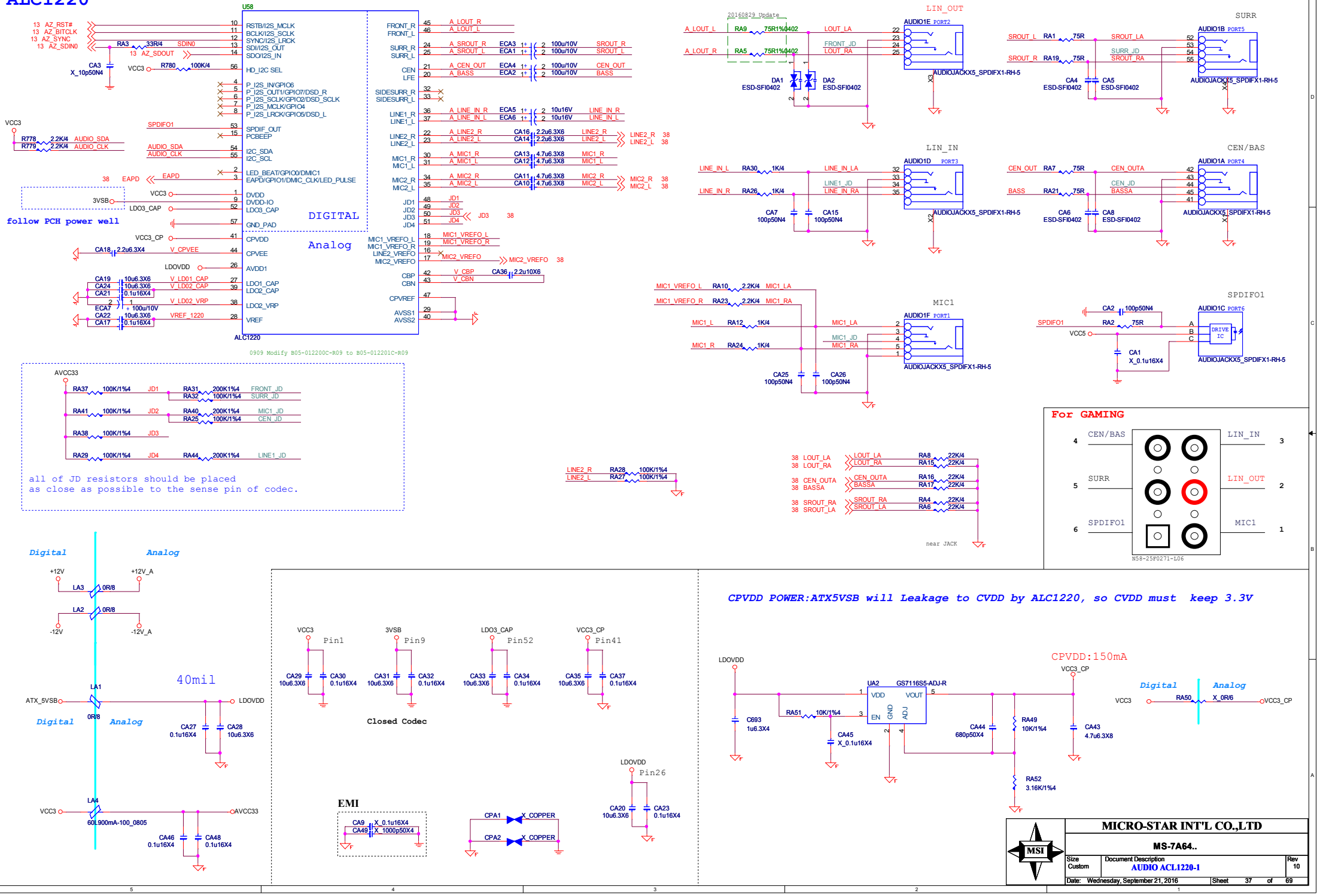
ALC1220


U58
ALC1220
DIGITAL
Analog
follow PCH power well
0909 Modify B05-012200C-R09 to B05-012201C-R09
all of JD resistors should be placed
as close as possible to the sense pin of codec.
LIN_OUT
SURR
LIN_IN
CEN/BAS
MIC1
SPDIFO1
For GAMING
CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V
CPVDD:150mA
Closed Codec
EMI
MICRO-STAR INT'L CO.,LTD
MS-7A64..
AUDIO ACL1220-1
Wednesday, September 21, 2016
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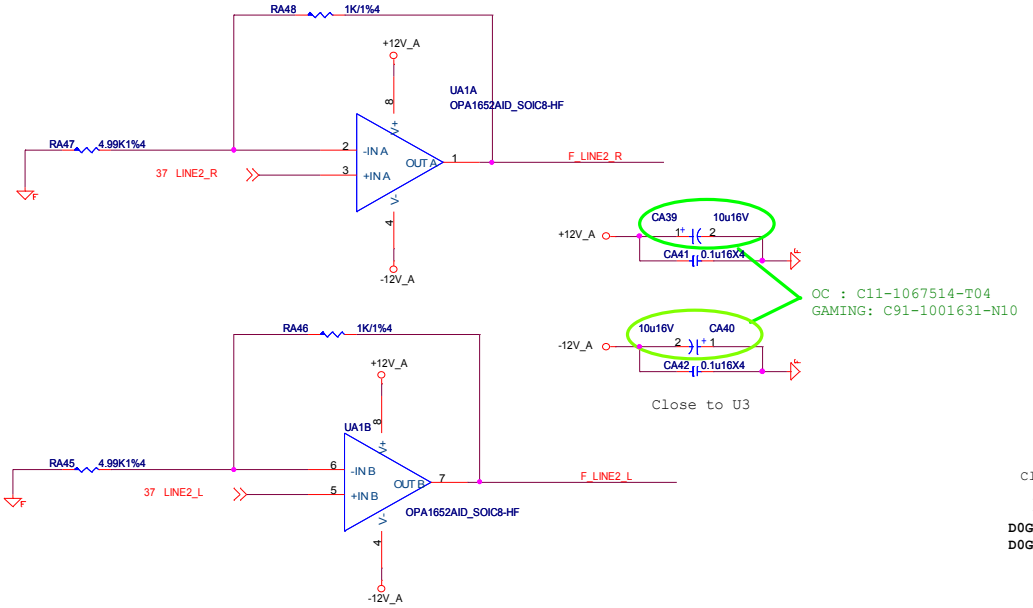
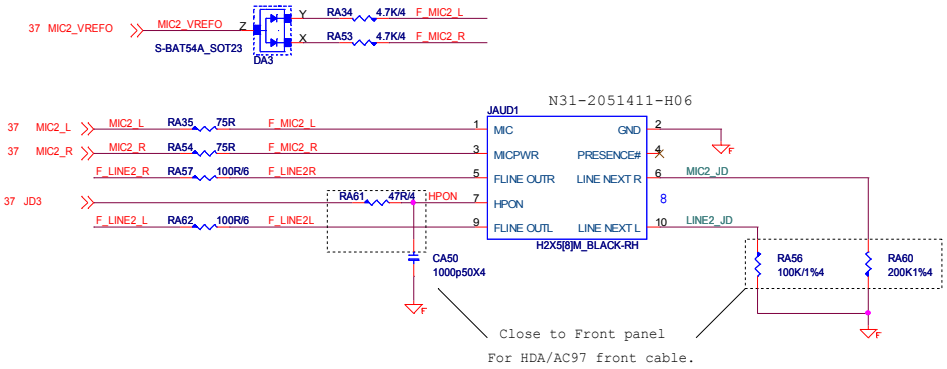


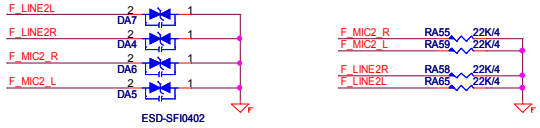


Close to Jack

ESD protect

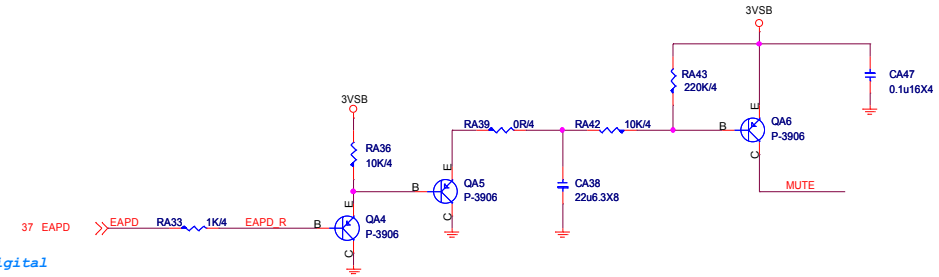
D0G-2710510-I05

D0G-2950500-SI0



Rear Line OUT De-POP circuit

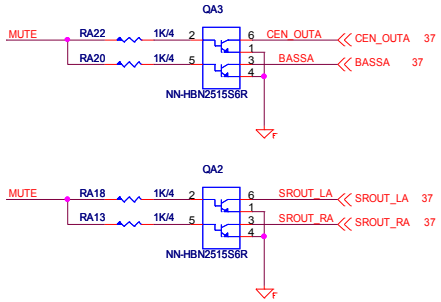
(De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA4,CA5, CA6, CA8,to TVS)



MICRO-STAR INT'L CO.,LTD

MS-7A64..

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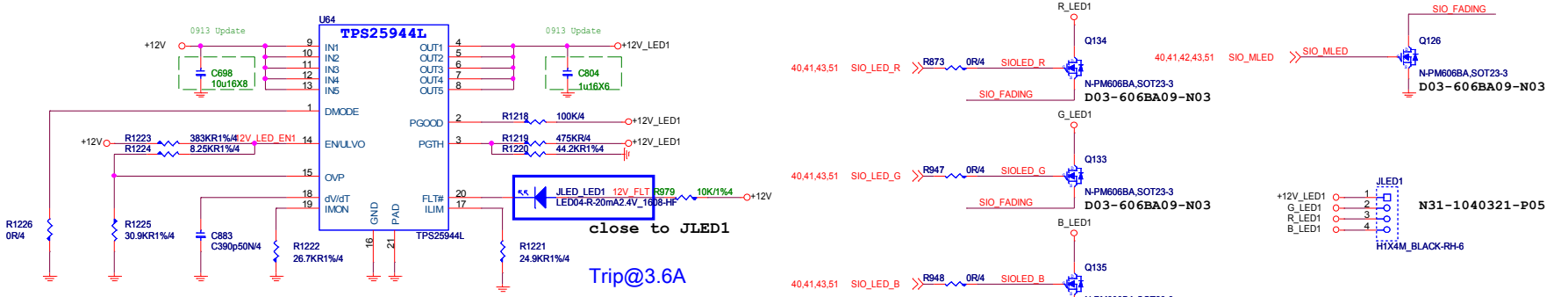
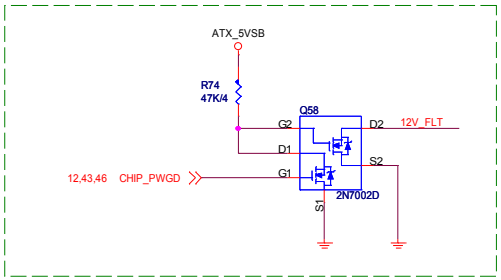
LED STRIPLINE

2016.07.12 change new design

外接LED 燈條 （RGB ）
---- PCB 文字面 （JLED1）
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 （12V/G/R/B） , 燈條總輸出電流限制為3安培 （12 伏特） ,
長度限制為2公尺 （待7A20驗證）

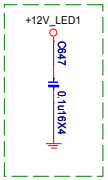


2016.08.31 ADD

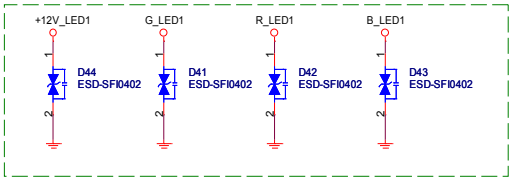


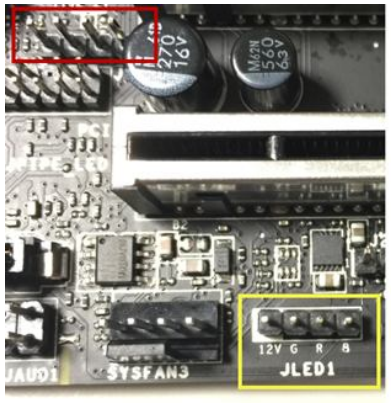
JLED1 CONNECTOR PN PLEASE CHECK PM

2016.08.02 ADD



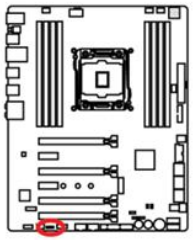
2016.08.02 Stuff ESD

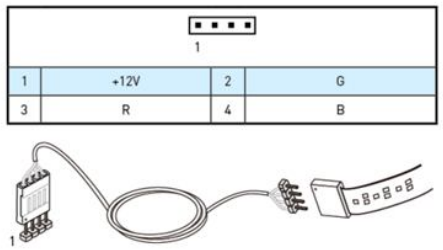




JLED1: RGB LED connector

This connector allows you to connect the RGB LED strip.

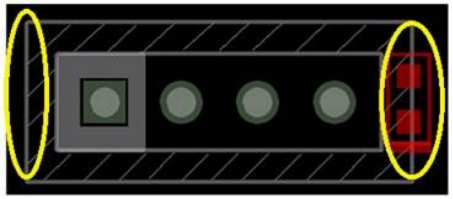




1	+12V	2	G
3	R	4	B

Important

- *This connector supports 5050 RGB multi-color LED strips (12V/G/R/B) with the maximum power rating of 3A (12V). Note that the length of the strip shall be no longer than 2 meters, or the LED brightness would become weak.*
- *Always turn off the power supply and unplug the power cord from the power outlet before installing or removing the RGB LED strip.*
- *Please use the **LED Effect** of GAMING APP to adjust, calibrate and control the LED light, refer to the Software section for details.*



JLED1電源警示燈請擺在旁側

MICRO-STAR INT'L CO.,LTD

MS-7A64..

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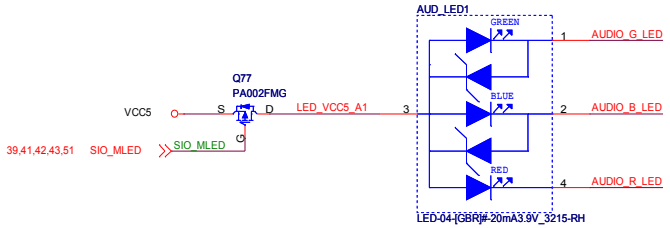
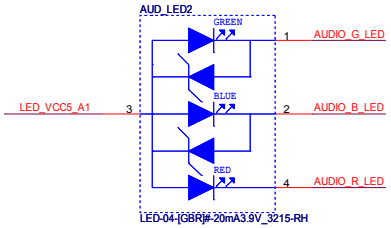
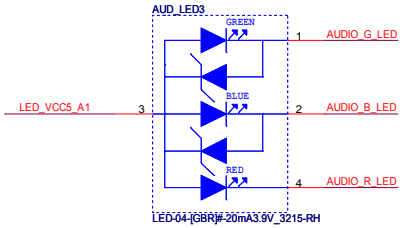
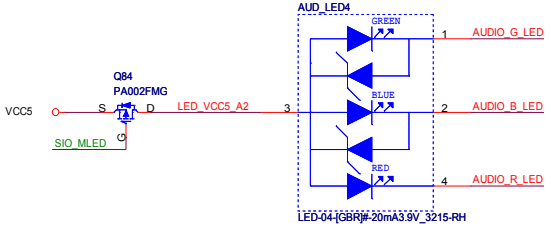
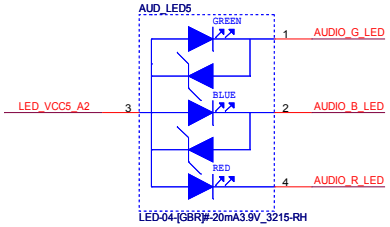
AUDIO_MOAT LED

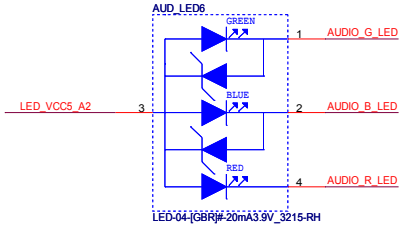


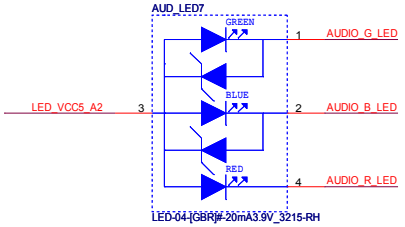


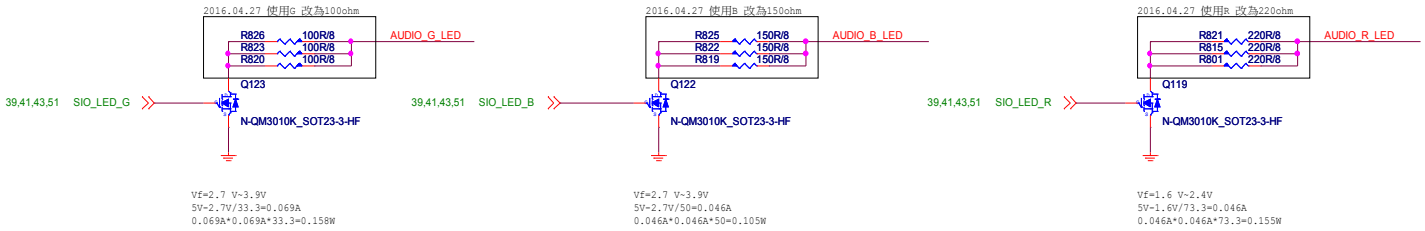












MICRO-STAR INT'L CO.,LTD

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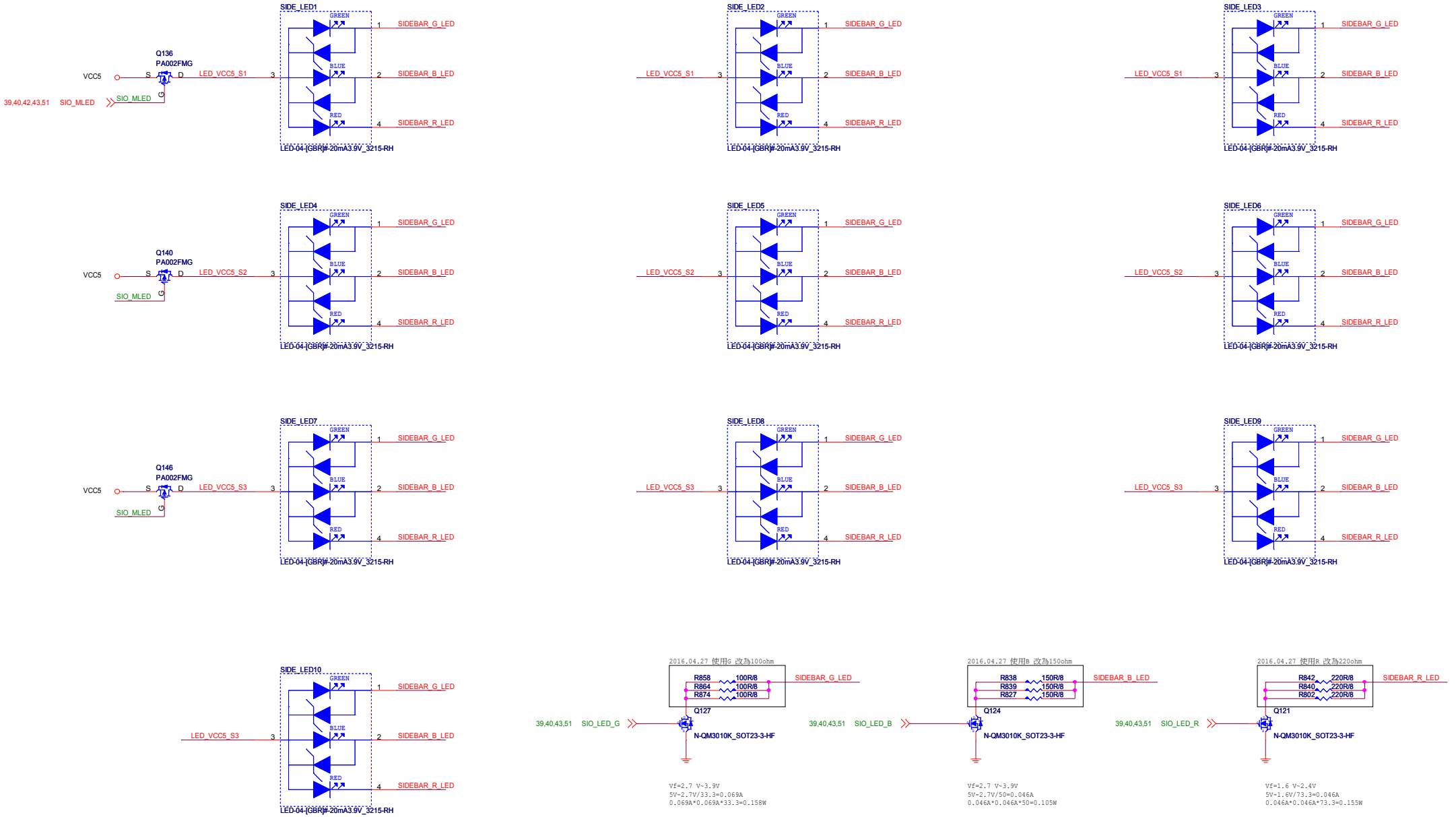
LED SIDEBAR

NEW FUNCTION



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
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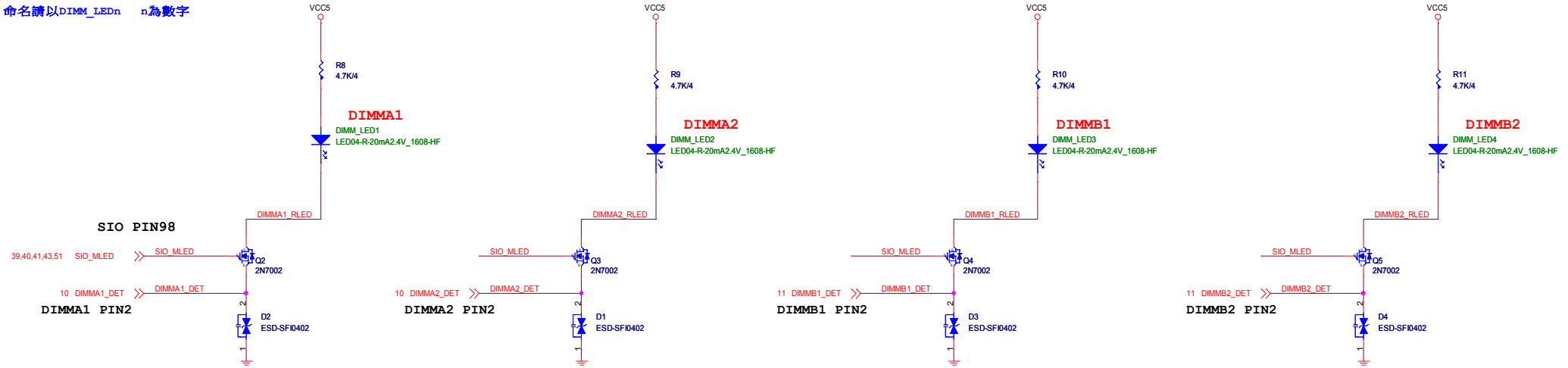
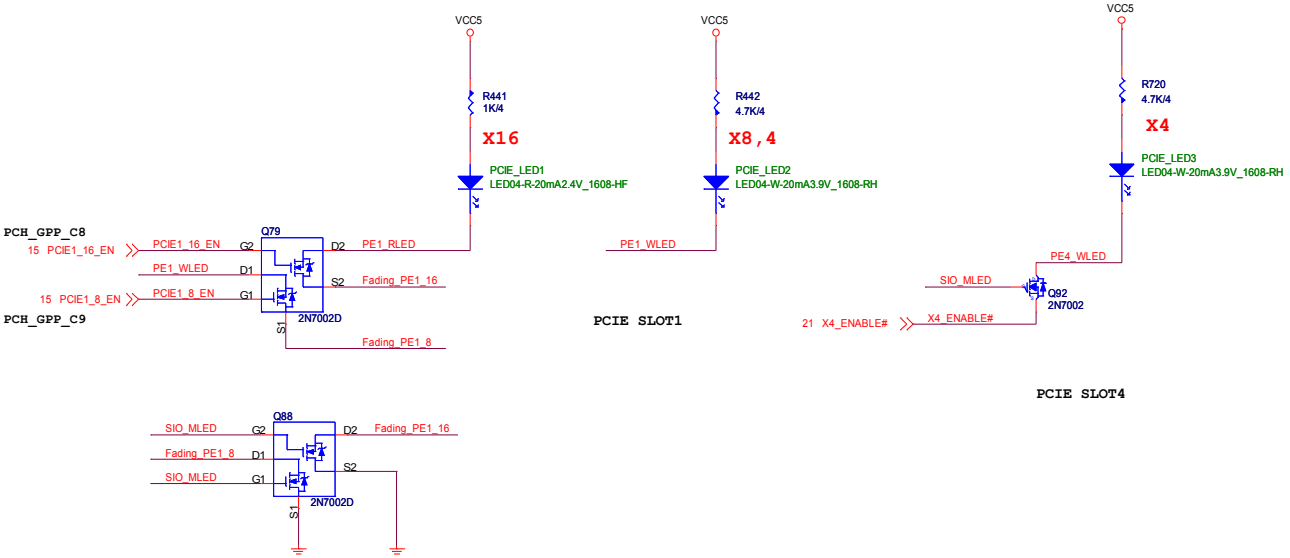
DIMM_SLOT

紅 : D0C-040P100-H91

LED 命名請以DIMM_LEDn n為數字

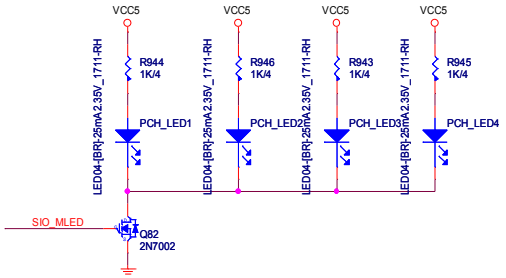


PCIE SLOT LED



PCH LED

NEW FUNCTION



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MS-7A64..

Size	Document Description	Rev
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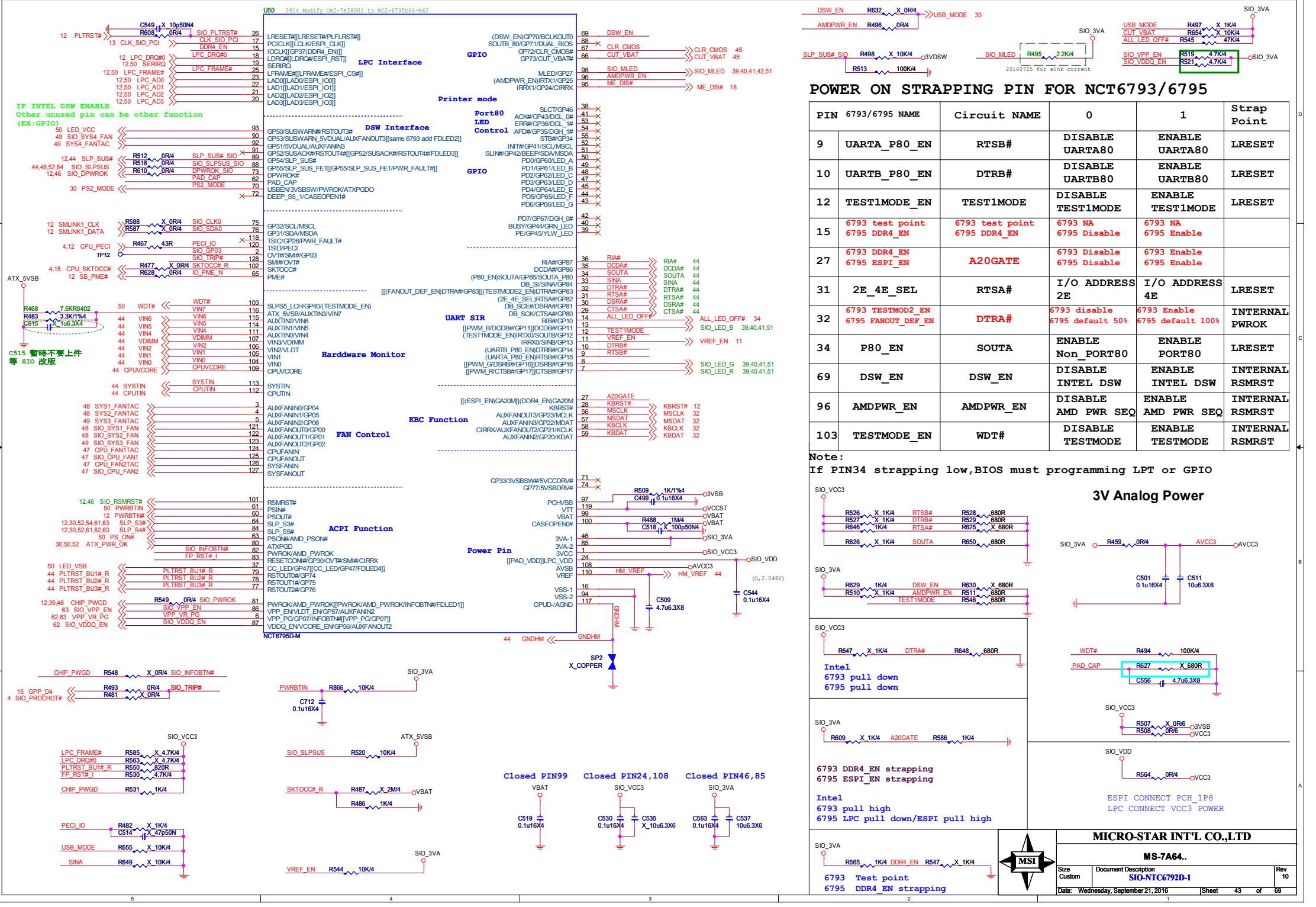

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

3V Analog Power

Intel
6793 pull down
6795 pull down

6793 DDR4_EN strapping
6795 ESPI_EN strapping

Intel
6793 pull high
6795 LPC pull down/ESPI pull high

6793 Test point
6795 DDR4_EN strapping

ESPI CONNECT PCH_1P8
LPC CONNECT VCC3 POWER

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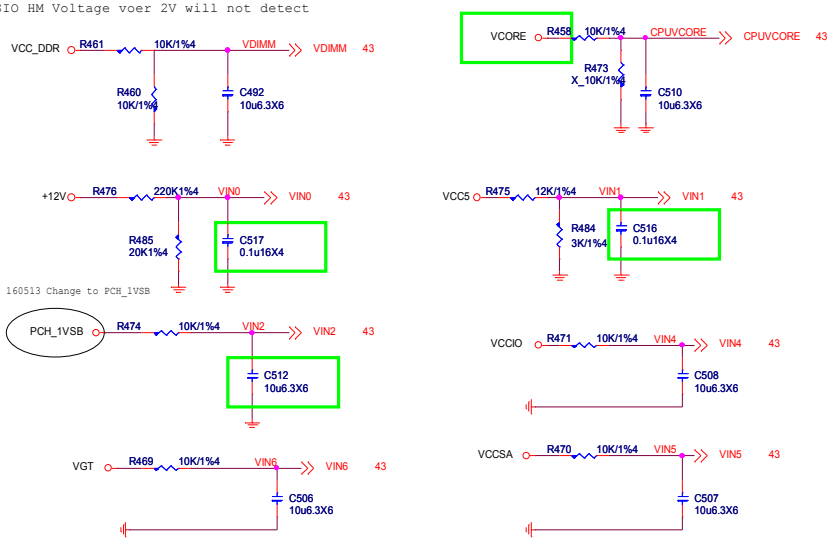
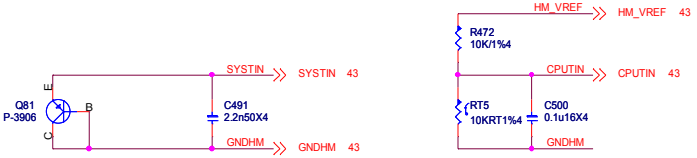
HW Monitor - Voltage

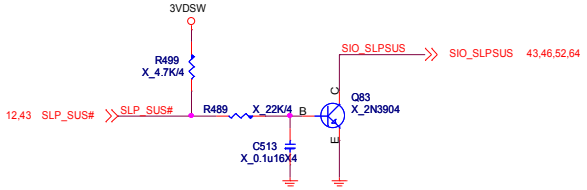
SIO HM Voltage voer 2V will not detect



Thermal Monitor

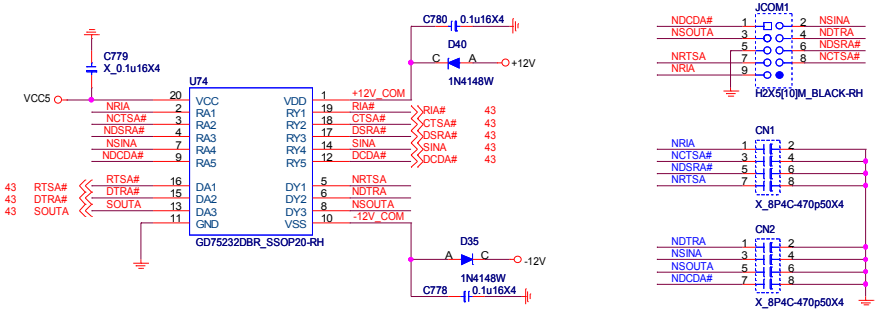


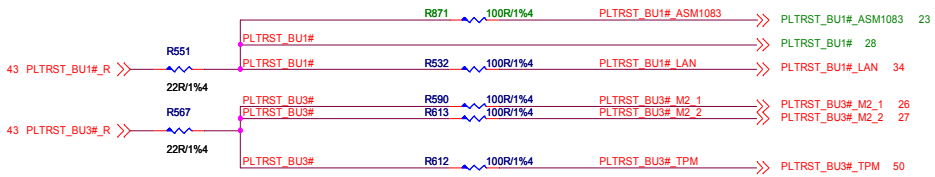
SLP_SUS Co-lay circuit

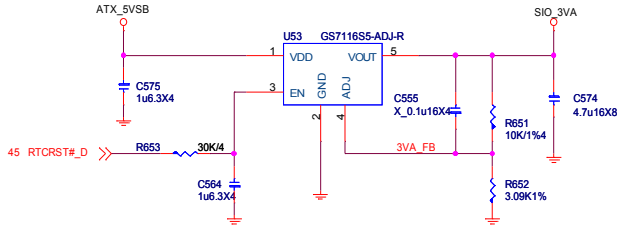


SERIAL PORT 1

NEW FUNCTION







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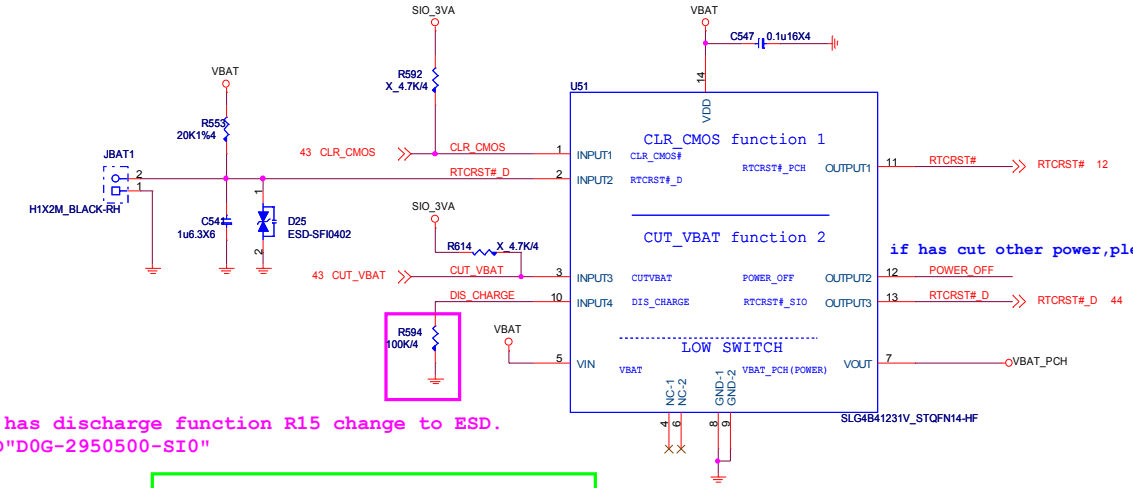
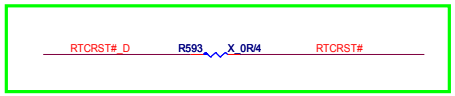
CLR_CMOS



if has cut other power,please use output 2.

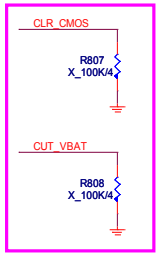
If has discharge function R15 change to ESD.
ESD"D0G-2950500-SI0"



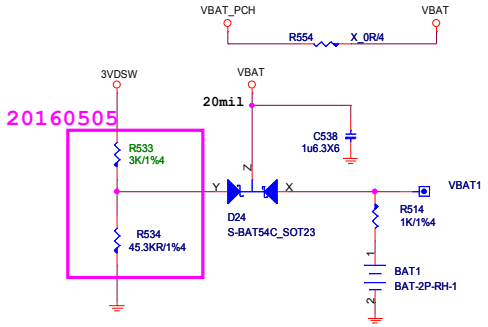
Co-Lay NOT USE U12 , R139 STUFF

If STUFF R139 Please Check RTCRST# Double Pull High

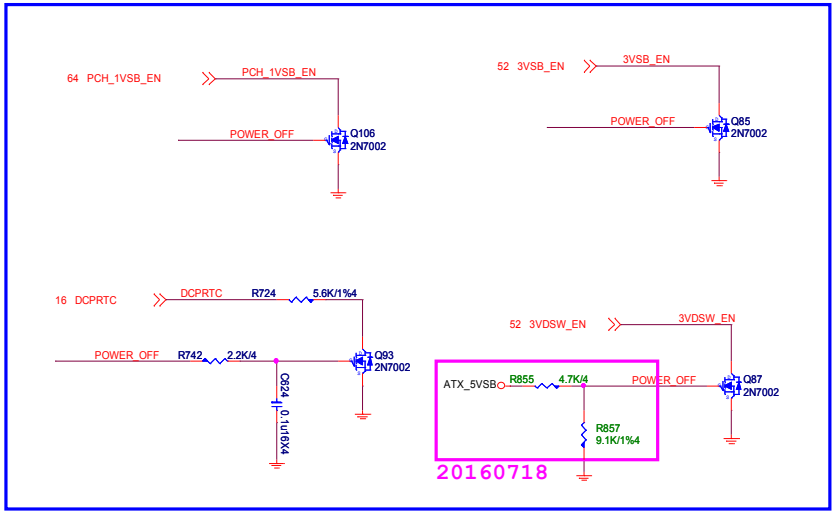
20160629



VBAT



Co-Lay NOT USE U12 , ALL UNSTUFF



Function 1		
IN		OUT
INPUT1	INPUT2	OUTPUT1
0	1	1
1	0	0
1	1	0
0	0	0

Default

Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

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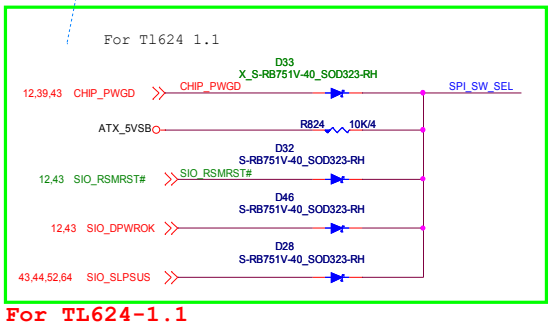
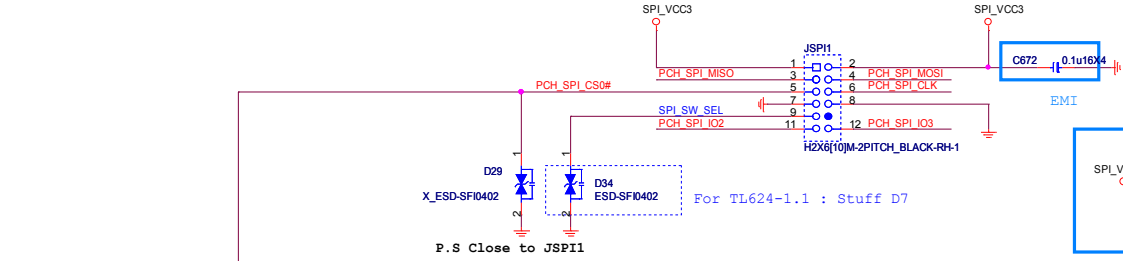
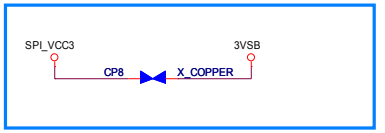
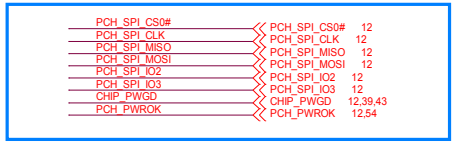
Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.



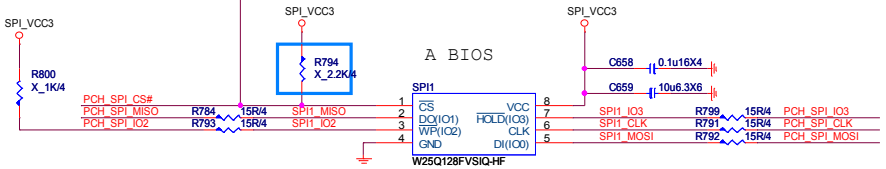
For TL624-1.1
SKYLAKE : Stuff D10/D17/R353
B85/H87 : Stuff D8/D9/R353
Others : Stuff R272







R795
0R/4
For TL624-1.1 : Stuff R62
Old : Don't stuff R62



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
Size: Custom	Document Description: BIOS	Rev: 10
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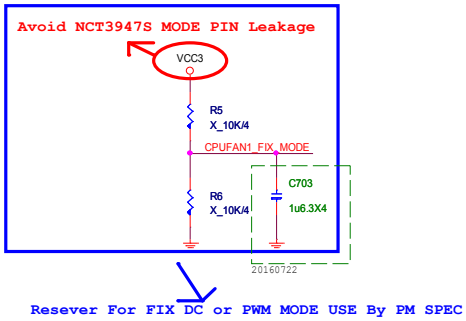
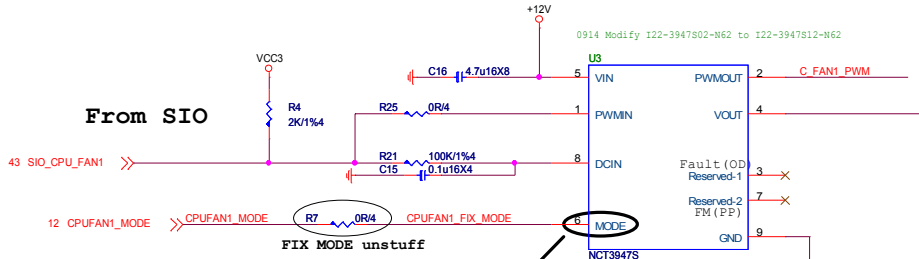
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

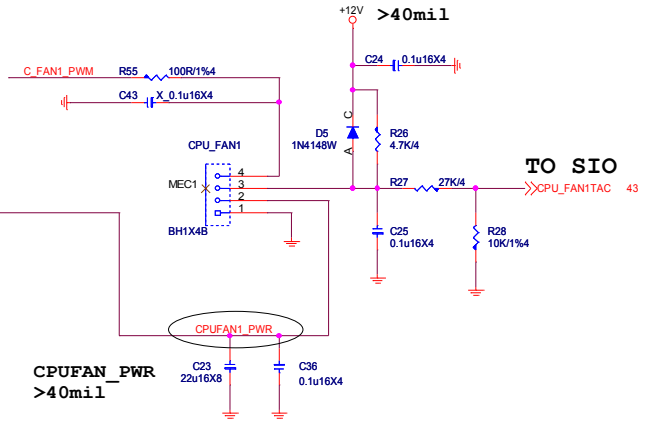




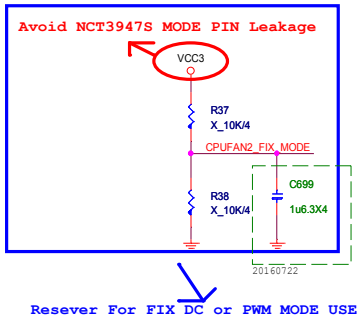
GPIO Control

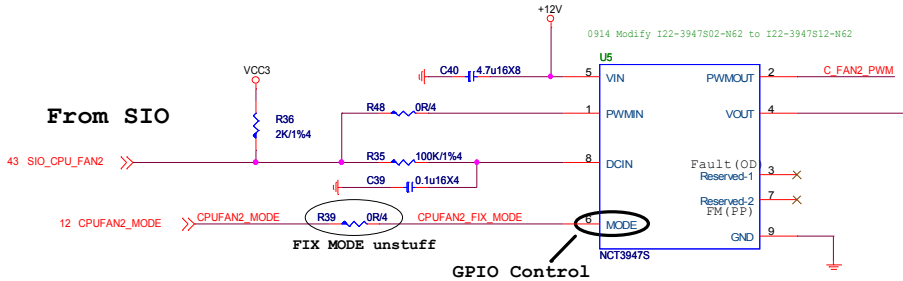
	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

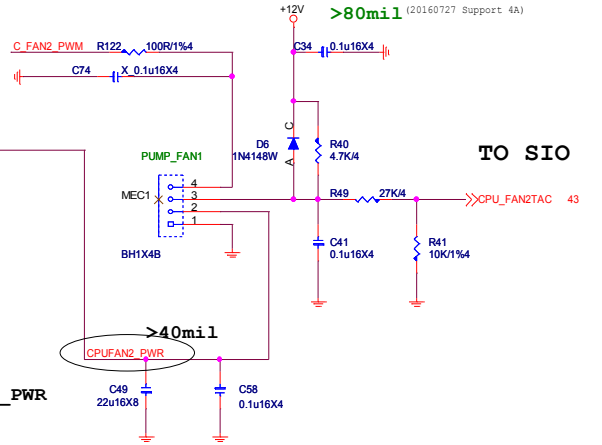




GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
2.FAULT : USE FAULT PIN Triger OVT/OCP Protection,LOW Atcive (Reserve NEW IC)
3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

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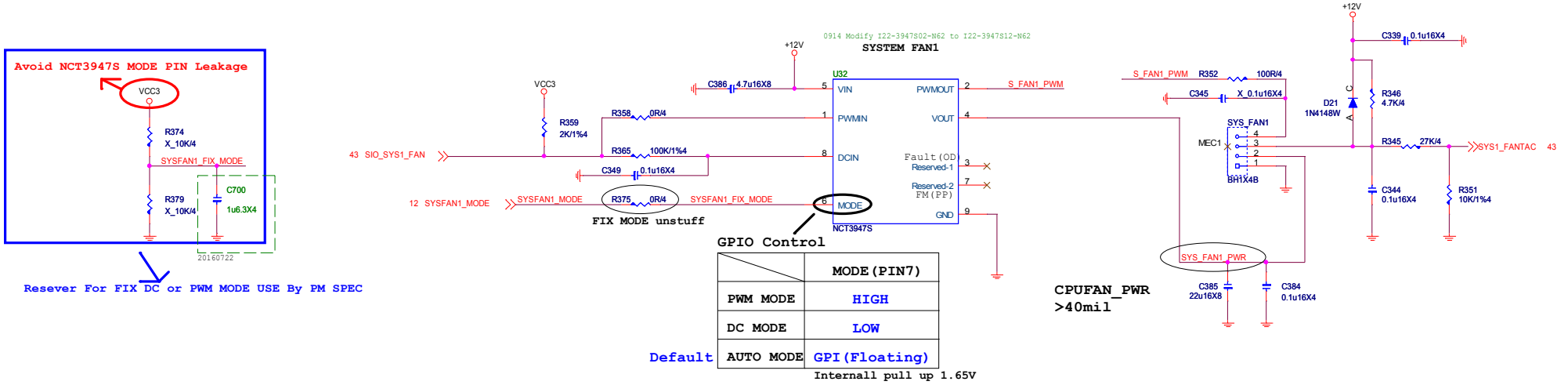
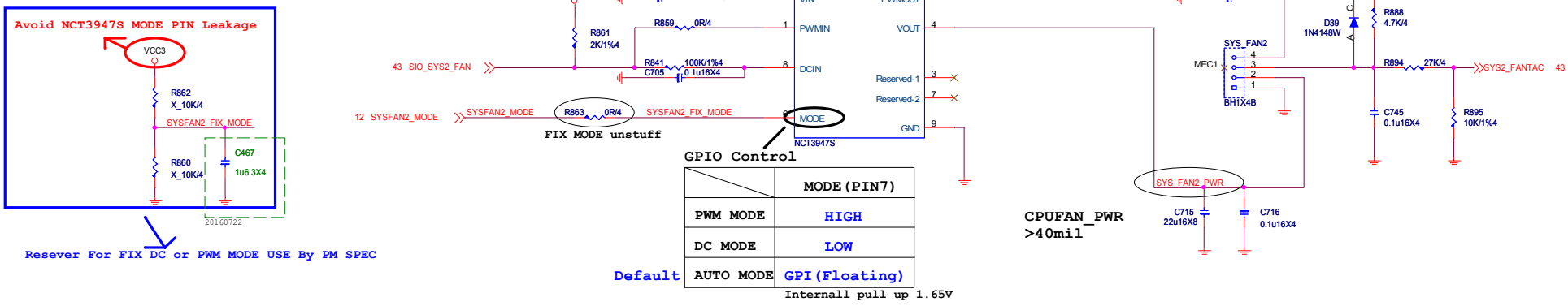
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	SYSTEM FAN1&2	10

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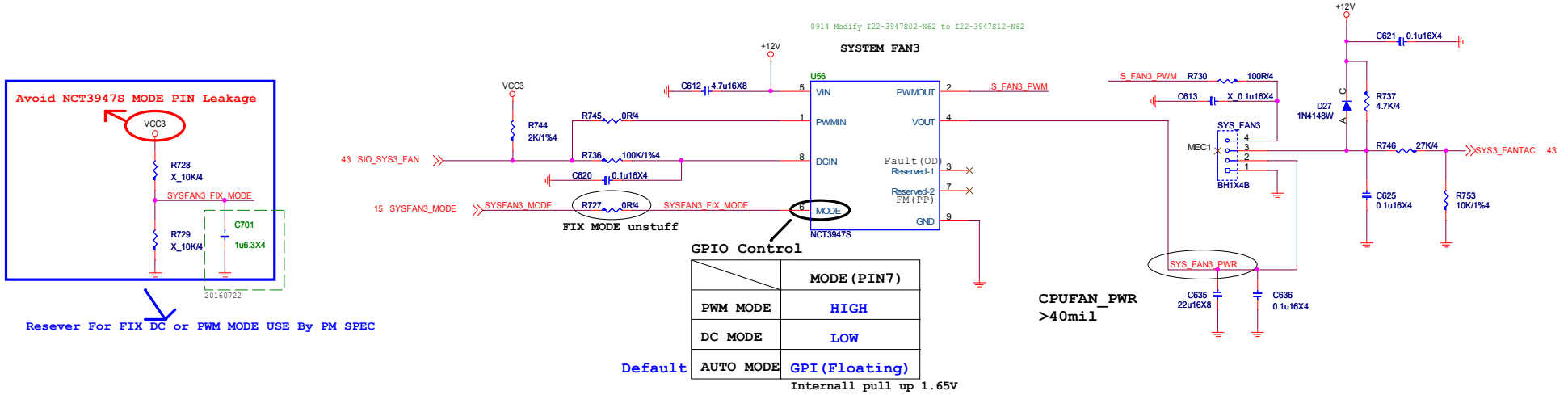
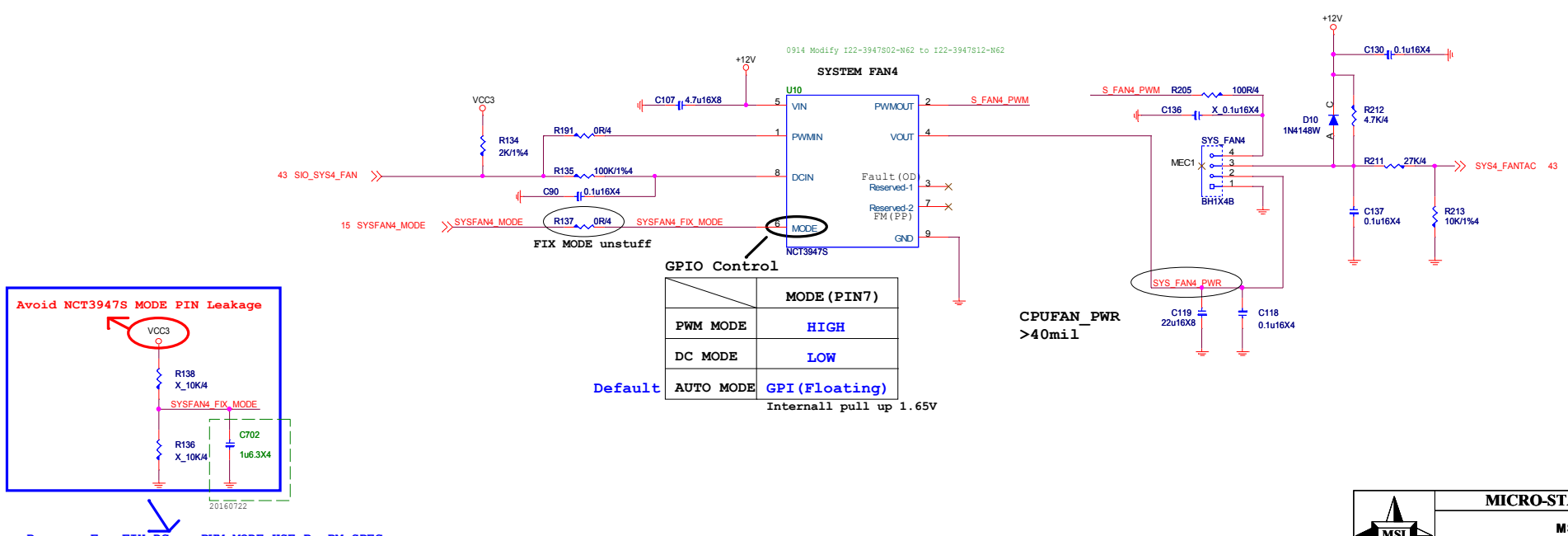
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



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Size: Custom	Document Description: SYSTEM FAN3&4
Rev: 10	
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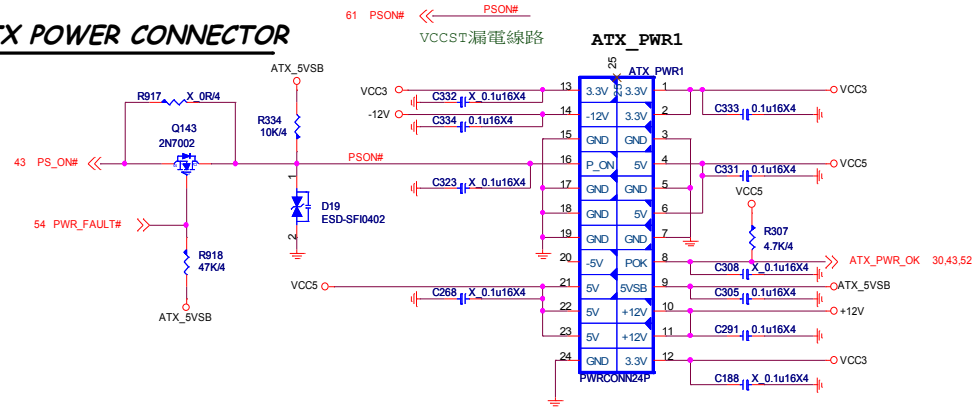
ATX POWER CONNECTOR



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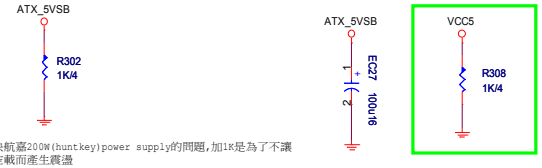
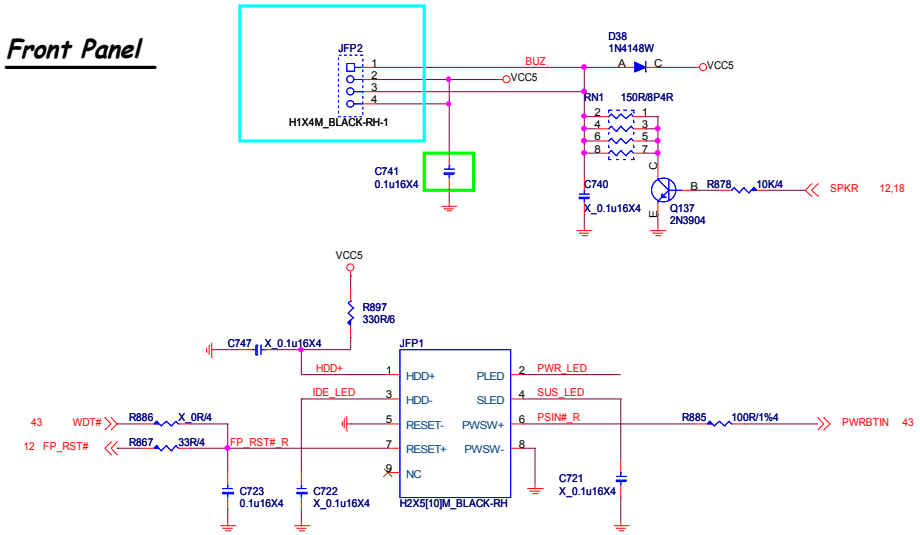
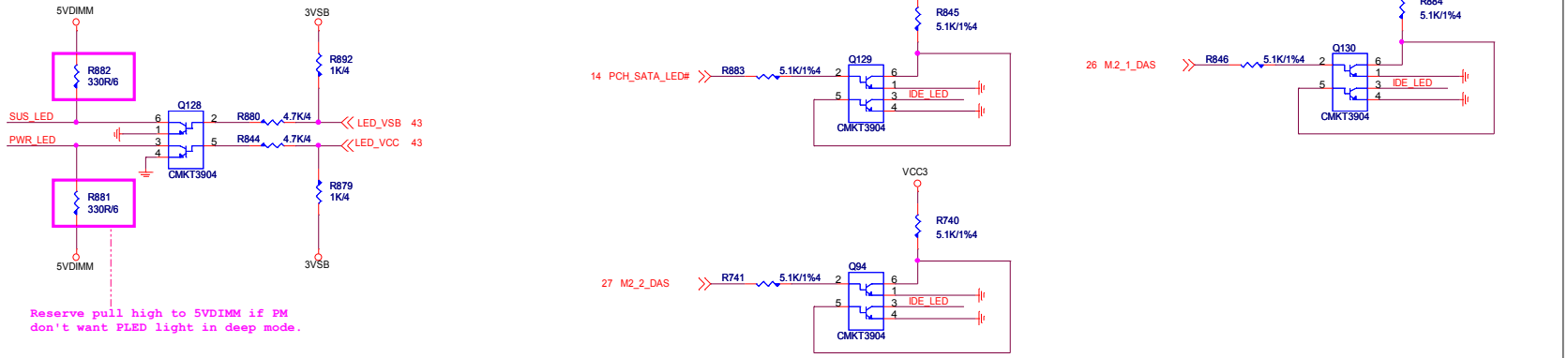


上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓ATX_5VSB空載而產生震盪

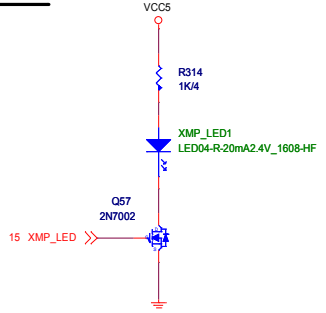
Front Panel



LED

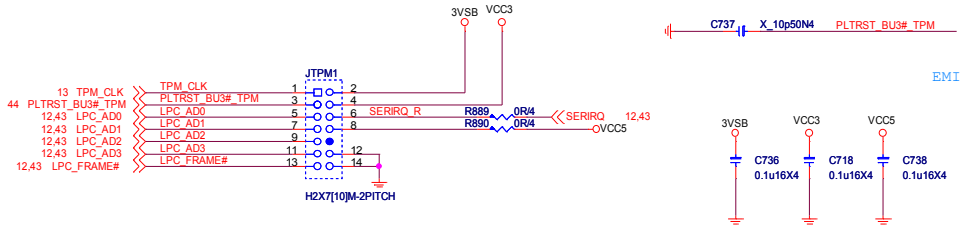


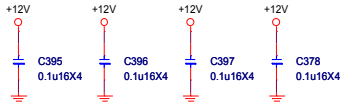
XMP LED



TPM

Confirm ESPI TPM card and TPM card pin difine
(Not ready)





MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	ATX Power/F_Panel	10

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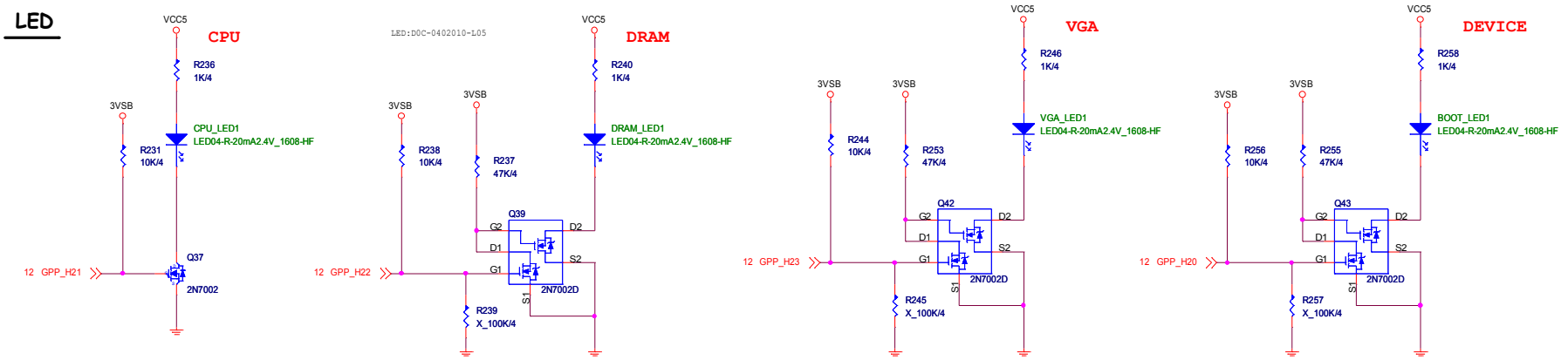
LED

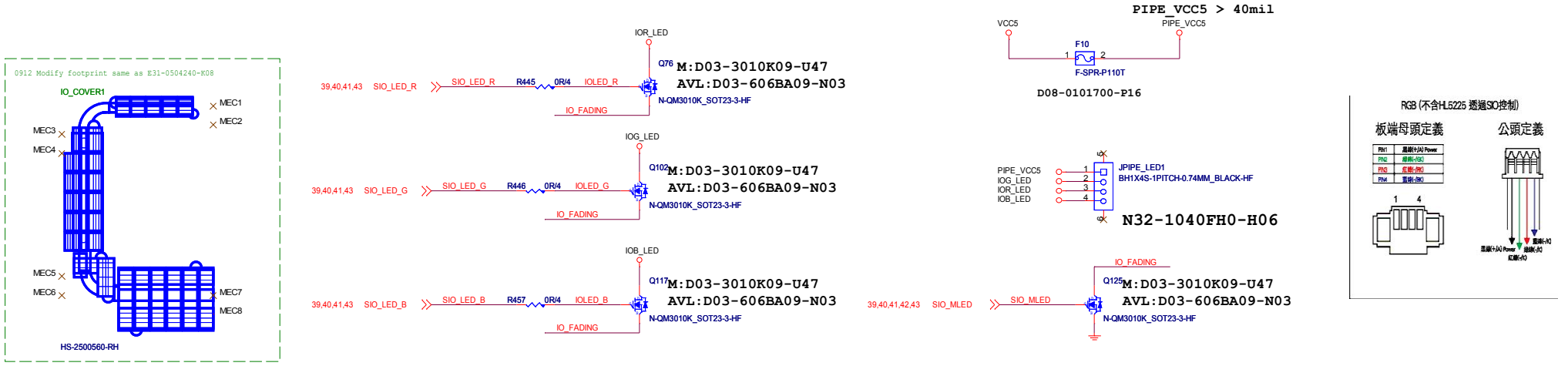


關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. 因此最後正常順利開機後，三個LED燈都是滅掉的。
   （系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

IO Cover + RGB LED



方案二 ： MCU Solutin 置於HS 背後需與國格討論 ， LED總功率算法 ：

--- 三色 ： GRB = 使用電壓 5V*0.06 電流 x 總燈數

--- 單色 ： G、B、W = 使用電壓 3V*0.02 電流 x 總燈數

--- 單色 ： R = 使用電壓 2V*0.02 電流 x 總燈數

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MS-7A64..

Size: Custom | Document Description: EZ DEBUG LED | Rev: 10

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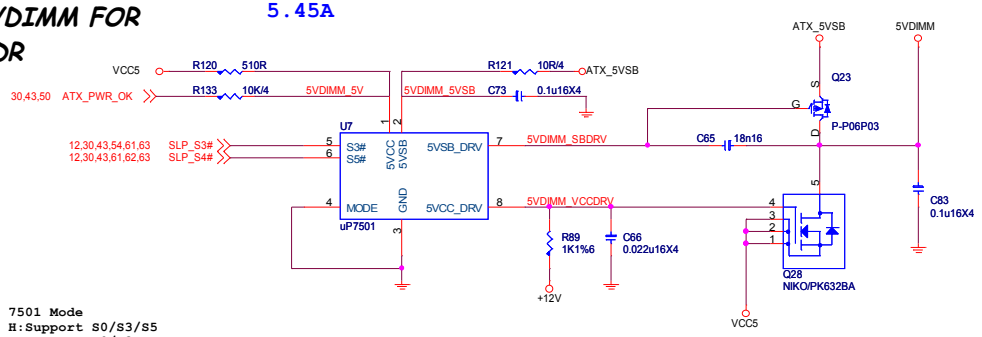
5VDIMM FOR DDR

5.45A

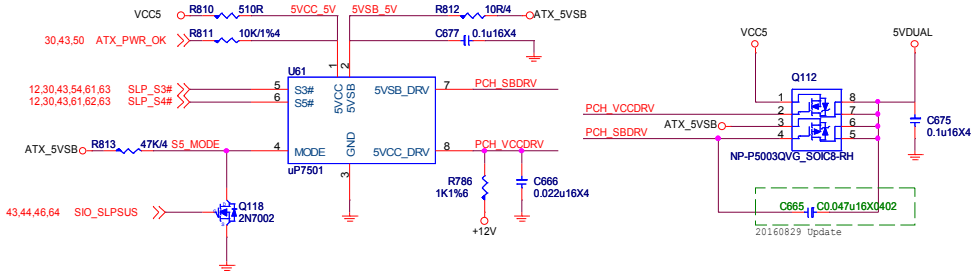


7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

5VDUAL

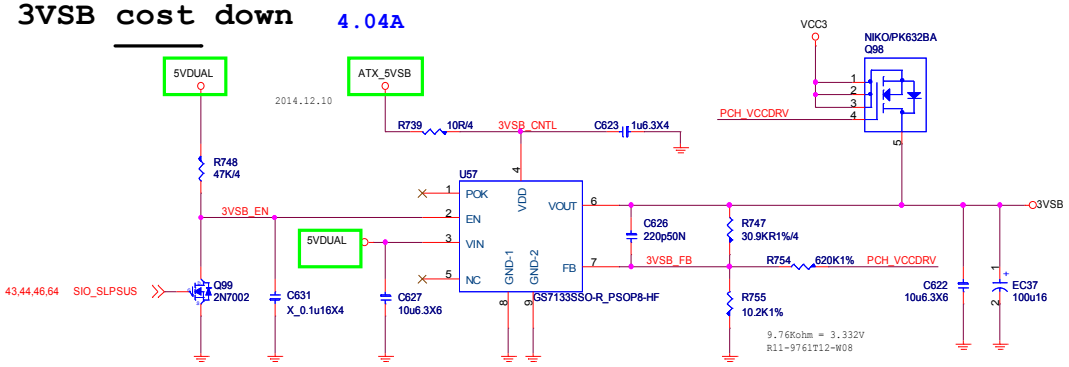
5VDUAL is power source of 1P0SB

PCH:2.95A
3VSB:4.04A
MAX:6.99A



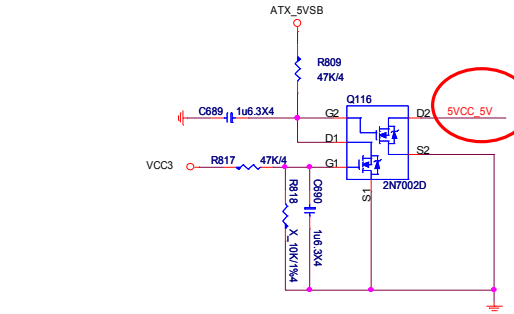
3VSB cost down

4.04A

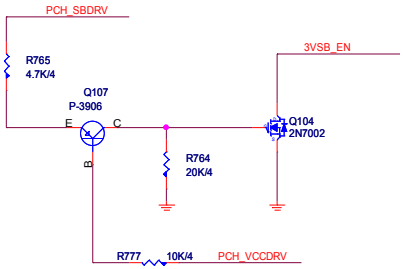


AVL:I31-3730S02-N62 2014.10.15 update

VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.



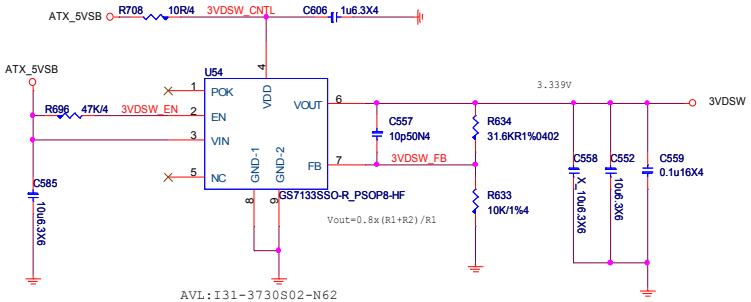
3VSB_EN → 3VSB_EN 45



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

3VDSW

0.422A



AVL:I31-3730S02-N62

3VDSW_EN → 3VDSW_EN 45

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Size	Document Description	Rev
Custom	ACPI UPI	10

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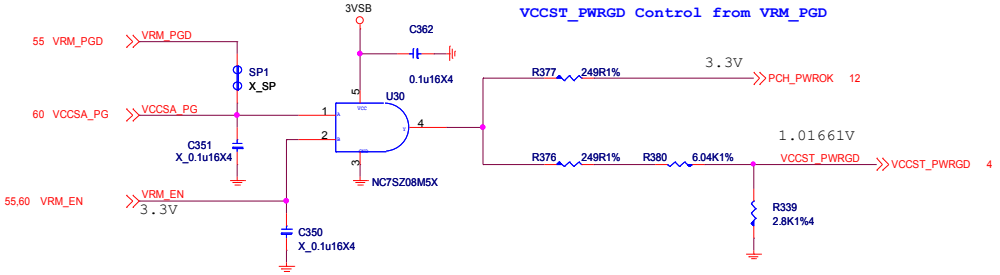
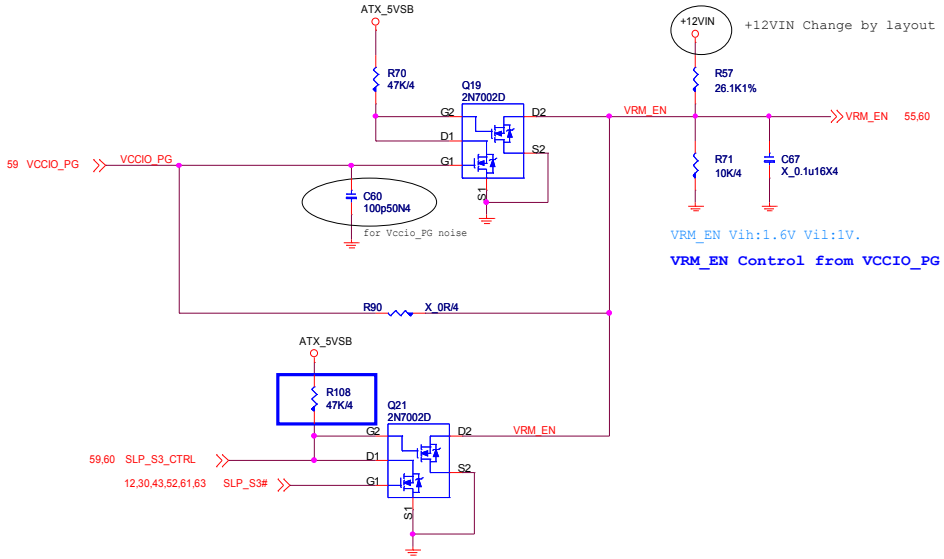
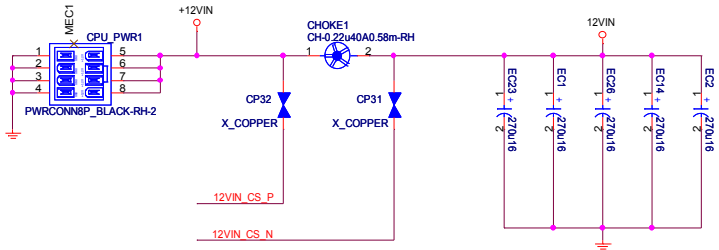
VCCSA&Vcore use same PWM IC, pull up VCC3
VCCSA&Vcore use different PWM IC,pull up VCCSA
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

PCH_PWROK Control from VCCIO_PG&VCCSA
VCCST_PWRGD Control from VRM_PGD

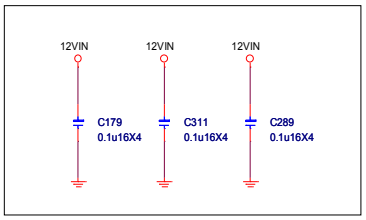


VRM_EN Control from VCCIO_PG

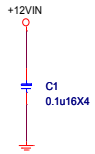




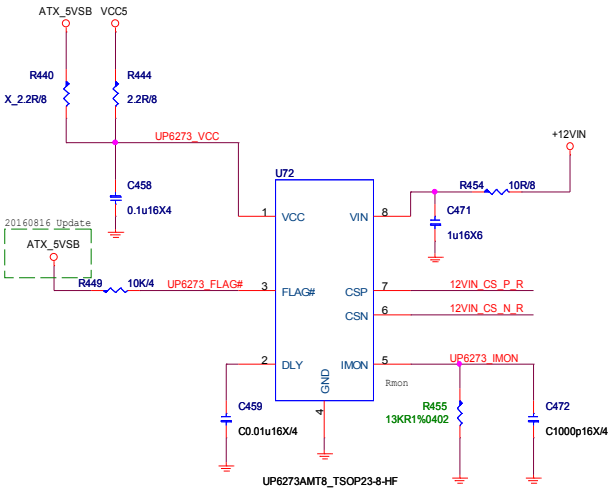
Iripple=30.95A
VCORE 18.101A
VGT 8.457A
VCCSA 4.392A



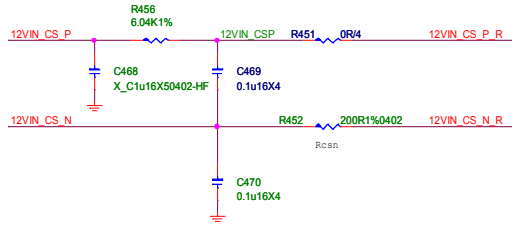
CLose to JPWR2



20160721 from RT9553A change to UP6273



RCSP x Cap = choke(L)/choke(DCR) x 1.1K
RCSP x 0.1 = 0.42/0.72 x 1.1K
RCSP = 6.41KR



RCSN = choke(DCR) / 10
RCSN = 72R

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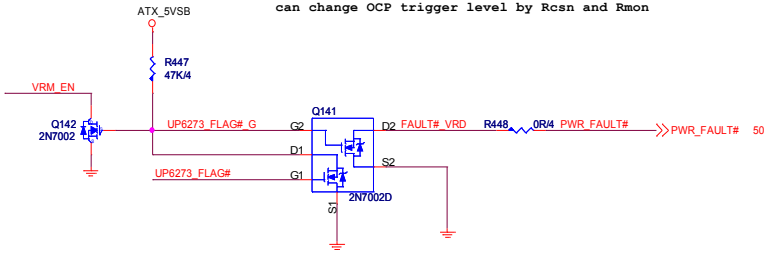
Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon



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MS-7A64..		
Size: Custom	Document Description: Rear I/O PS2	Rev: 10
Date: Tuesday, September 20, 2016	Sheet 53 of 69	

Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 200A

VGT: ICC Max 48A
LL: 3.1 mohm
OCP: 75A

0906 Modify OI3-7A16002 to I32-9508Q0C-U33

U8

VCC5 R162 2.2R/1%6 V_9508 C101 1u16X6 → VCC (20)

PSYS (44)

58 PWM1A → PWM1A (46)

56 PWM2A → PWM2A (47)

R80 12K/1%4 → PROG3 (48)

20160729 modify

58 CSP1A → CSP1A (37)

CSN1A_R → CSN1A (38)

V_9508 R113 1K/1%4

56 CSP2 CSP2 R102 9.1K/1%4 → CSP2_R → CSP2A (39)

56 CSN2 CSN2 R84 220R/1%4 → CSN2_R → CSN2A (40)

C64 0.1u16X4

C53 0.1u16X4

CSPA (35)

CSNA (34)

FBA (32)

58 CSP1A-1 CSP1A-2 CSN1A-1 CSN1A-2

CSP1A-1 R129 3.3KR1%

CSP1A-2 R131 3.3KR1%

for transient undershoot fine tune

R130 2K/1%4

R127 191R1%0402-HE CSNA

R128 10K/1%4

C77 C0.22u16X4 C78 C0.22u16X4 C79 C0.047u16X0402

NTCA_Lb R116 X_0R/4 NTCA_La

C80 0.1u16X4

R145 0R/4 C86 1000p50X4 → COMPA (33)

EAPA (31)

DACA (30)

CSN1A-1 R147 10R1%4

CSN1A-2 R149 10R1%4

FBRTNA (29)

C87 X_0.1u16X4 R148 1K/1%4 FBA

C105 X_0.1u16X4

C113 680p50X4 IMON_A → IMONA (28)

R202 220R/1%4 R184 32.4K/1%4

R115 220R/1%4 R114 32.4K/1%4 → ISUMA (36)

12VIN

R201 0R/4

C112 0.1u16X4

R83 39K/1%4 → TONSET (42)

VINSEN (19)

R61 X_0R/4 → PROG1 (51)

R62 16.5KR1%0402-EM → PROG2 (50)

20160729 modify

TSENSE (43)

TSENSEA (41)

GND (53)

uP9508

R163 220R/1%4 R146 3K/1%4 EAPA

C102 X_0.1u16X4

DACA

4 VGT_VCC_SENSE R164 0R/4

VGT R150 100R/1%4

C104 X_0.1u16X4

C114 X_0.1u16X4 C103 0.01u25X4 FBRTNA

4 VGT_VSS_SENSE R185 0R/4

R186 100R/1%4

NTC1a R66 7.32K1%4 C63 0.1u16X4 R82 0R/4 TSENSE

NTCA1a R67 7.32K1%4 C52 0.1u16X4 R85 0R/4 TSENSEA

ATX_5VSB R69 47K/4 R68 47K/4

Q18 2N7002D G2 D1 G1 D2 S2 S1

R63 44.2KR1%4 PROG2

J1 H1X2M-2PITCH_BLACK-HF JVBOOT

D7 ESD-SSF0402

DRCTRL (49) → R79 DRCTRL 56,57,58

R98 10K/1%4 1K/1%4

PCB layout notice: DRCTRL trace is noise sensitive, keep >15mil space to other net

PWM1 (52) → PWM1 56

PWM2_IMAXA → PWM2_IMAXA 57

R95 48.7K/1%4

PWM3_IMAX → PWM3_IMAX 57

R96 100K/1%4

20160729 modify

CSP1 (9) CSP1_R R125 9.1K/1%4 → CSP1 56

CSN1 (8) CSN1_R R126 220R/1%4 C76 0.1u16X4 C75 0.1u16X4 → CSN1 56

CSP2 (7) CSP3_R R111 9.1K/1%4 → CSP3 57

CSN2 (6) CSN3_R R112 220R/1%4 C69 0.1u16X4 C68 0.1u16X4 → CSN3 57

CSP3 (5) CSP4_R R93 9.1K/1%4 → CSP4 57

CSN3 (4) CSN4_R R94 220R/1%4 C62 0.1u16X4 C61 0.1u16X4 → CSN4 57

CSP (12) CSP_R

CSN (11) CSN_R R144 150R1%4

FB (14) C98 X_0.1u16X4 R173 1K/1%4 R210 0R/4 R209 100R/1%4 VCORE_VCC_SENSE 4 VCORE C124 X_0.1u16X4 FBRTN

COMP (13) R172 0R/4 C122 1000p50X4

C85 0.1u16X4

EAP (15) EAP R174 5.76K/1%4 R198 510R1%0402 C123 X_0.1u16X4

0906 Modify for Vendor suggestion

DAC (16) DAC C99 0.01u25X4

FBRTN (17) R199 0R/4 VCORE_VSS_SENSE 4 C111 X_0.1u16X4 R175 100R/1%4 CP18 X_COPPER

IMON (18) IMON C100 680p50X4 R176 39K/1%4 R200 7.5KR1%0402

ISUM (10) ISUM R142 39K/1%4 R141 7.5KR1%0402

0906 Modify for Vendor suggestion

SCL (21) SMBCLK_9508

SDA (22) SMBDATA_9508

20160729 modify

VRHOT# (23) H_PROCHOT# H_PROCHOT# 4

SYSFAULT# (45) SYSFAULT# R101 10K/1%4 VCC5

VR_RDY (3) VRM_PGD VRM_PGD 54

SDIO (26) VIDSOUT R181 10R1%4 H_VIDSOUT

ALERT# (25) VIDALERT# RC3 0R/4 H_VIDALERT#

SCLK (24) VIDSCLK R178 49.9R1%4 H_VIDSCLK

close to VRM < 0.1"

EN (27) VRM_EN VRM_EN 54,60

20160729 modify

20160729 modify

R124 4.99KR1% CSP1

R72 4.99KR1% CSP2

R110 4.99KR1% CSP3

R92 4.99KR1% CSP4

R171 1.47KR1%4

NTC_Lb R170 X_0R/4 NTC_La

R143 10K/1%4 C97 0.47u16X6 C96 0.33u16X6 C95 C82000p16X

0906 Vendor suggestion

R123 10R1%4 CSN1

R73 10R1%4 CSN2

R109 10R1%4 CSN3

R91 10R1%4 CSN4

VCCST

close to VRM <0.1"

R179 45.3R1% H_VIDSCLK 4

R182 100R/1%4 H_VIDSOUT 4

R180 X_100R/1%4 H_VIDALERT# 4

C132 1u6.3X4 C125 0.1u16X4

直接放在R1105,R1080,R1029旁邊

8,12 SMBDATA_VCC 8,12 SMBCLK_VCC RC2 0R/4 RC1 0R/4 SMBDATA_9508 SMBCLK_9508

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MS-7A64..

Size	Document Description	Rev
Custom	PWM-UP9508 VCORE+VGT	10

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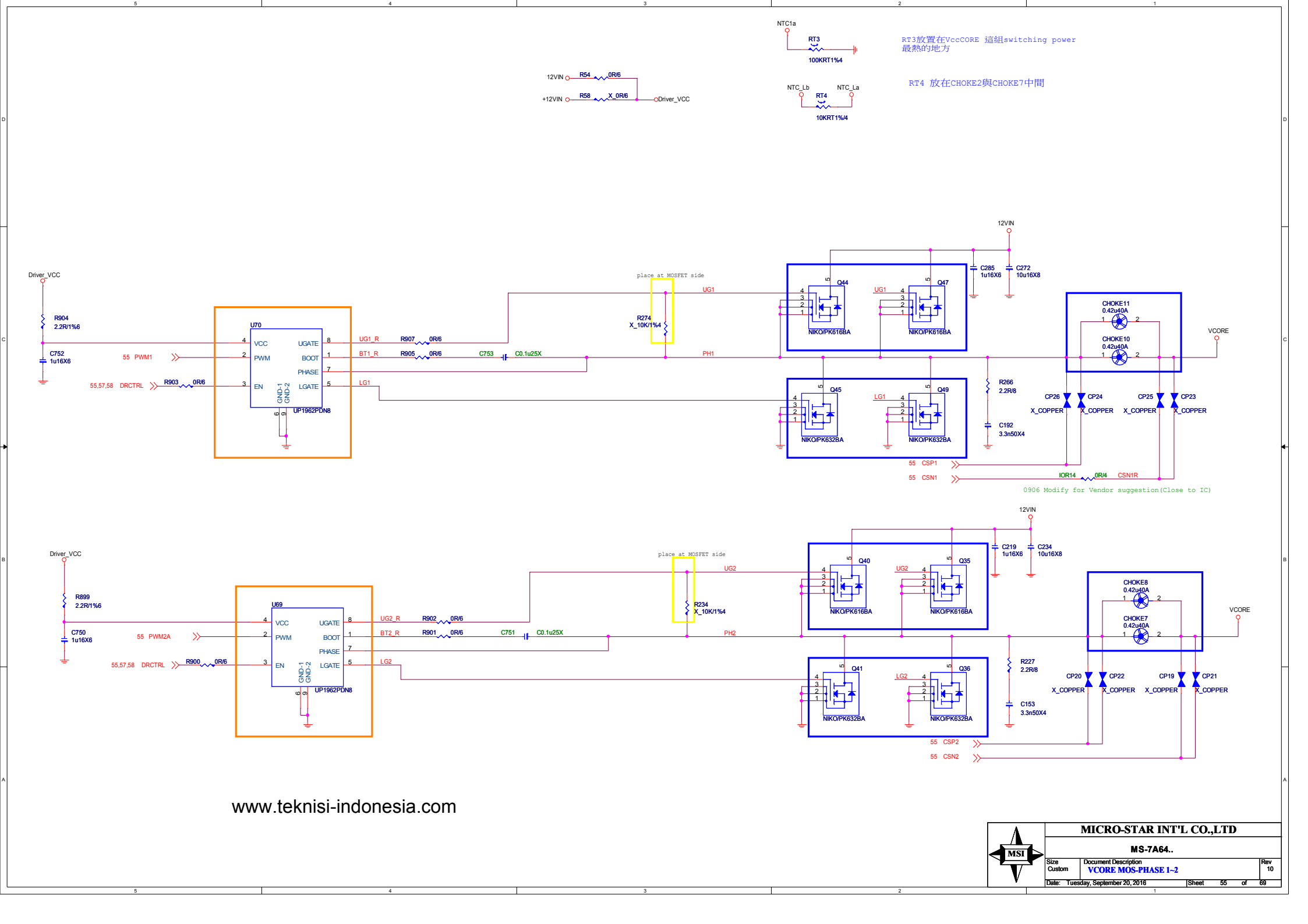

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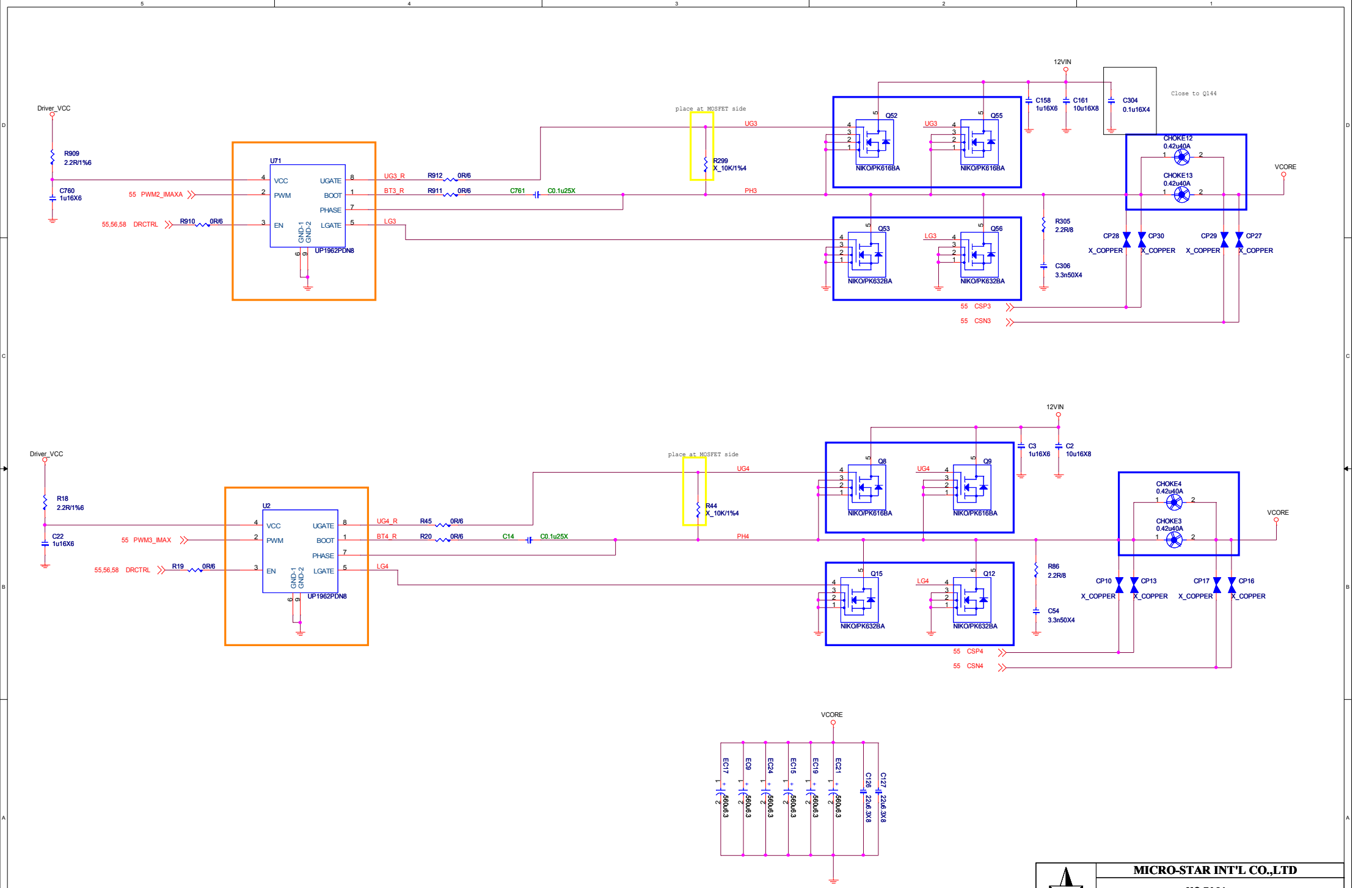
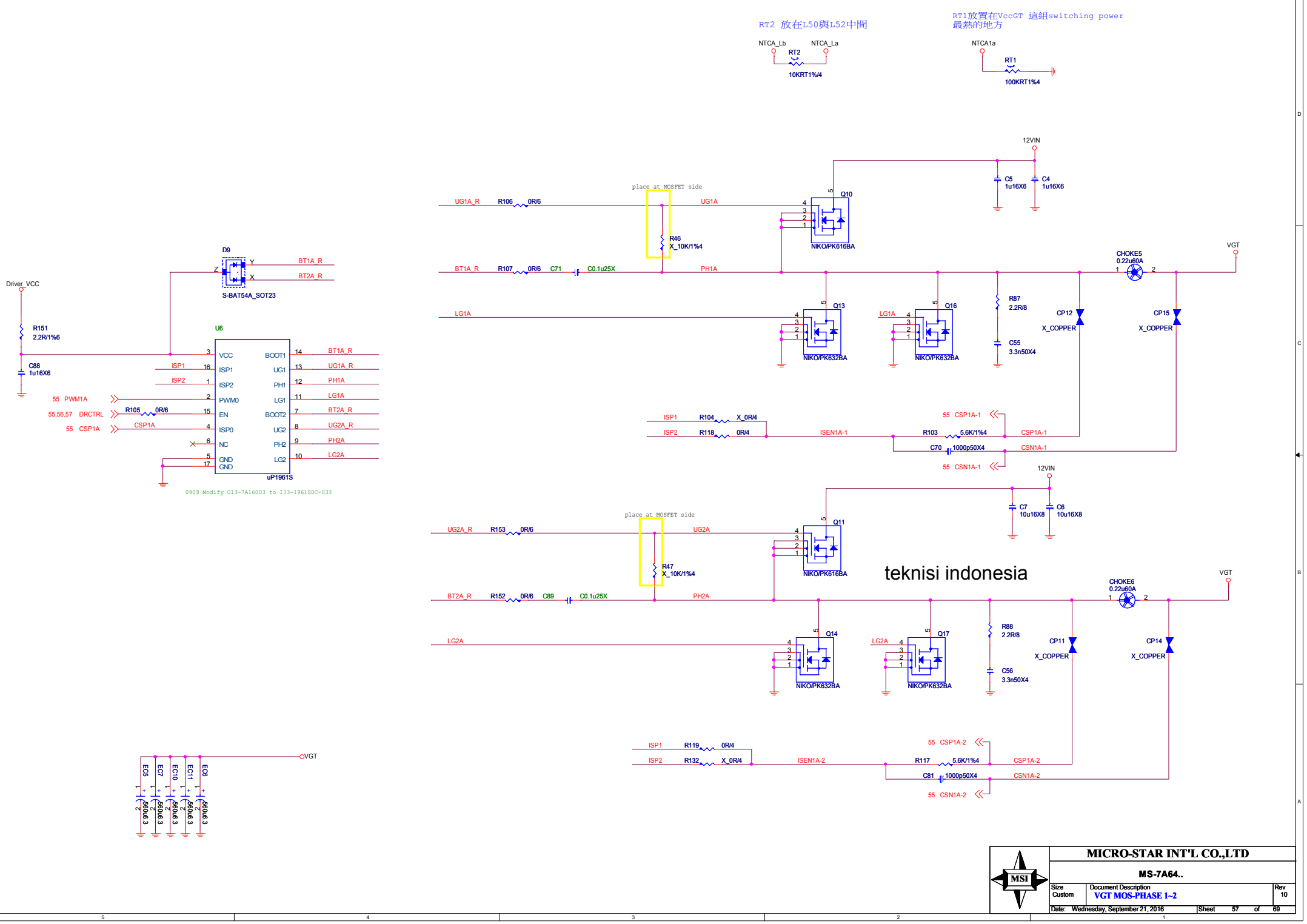
MS-7A64..

Size	Document Description	Rev
Custom	VCORE MOS-PHASE 1~2	10

Date: Tuesday, September 20, 2016 Sheet 55 of 69



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7A64..	
Size: Custom	Document Description: VCORE MOS-PHASE 3~4	Rev: 10
Date: Tuesday, September 20, 2016	Sheet 56 of 69	



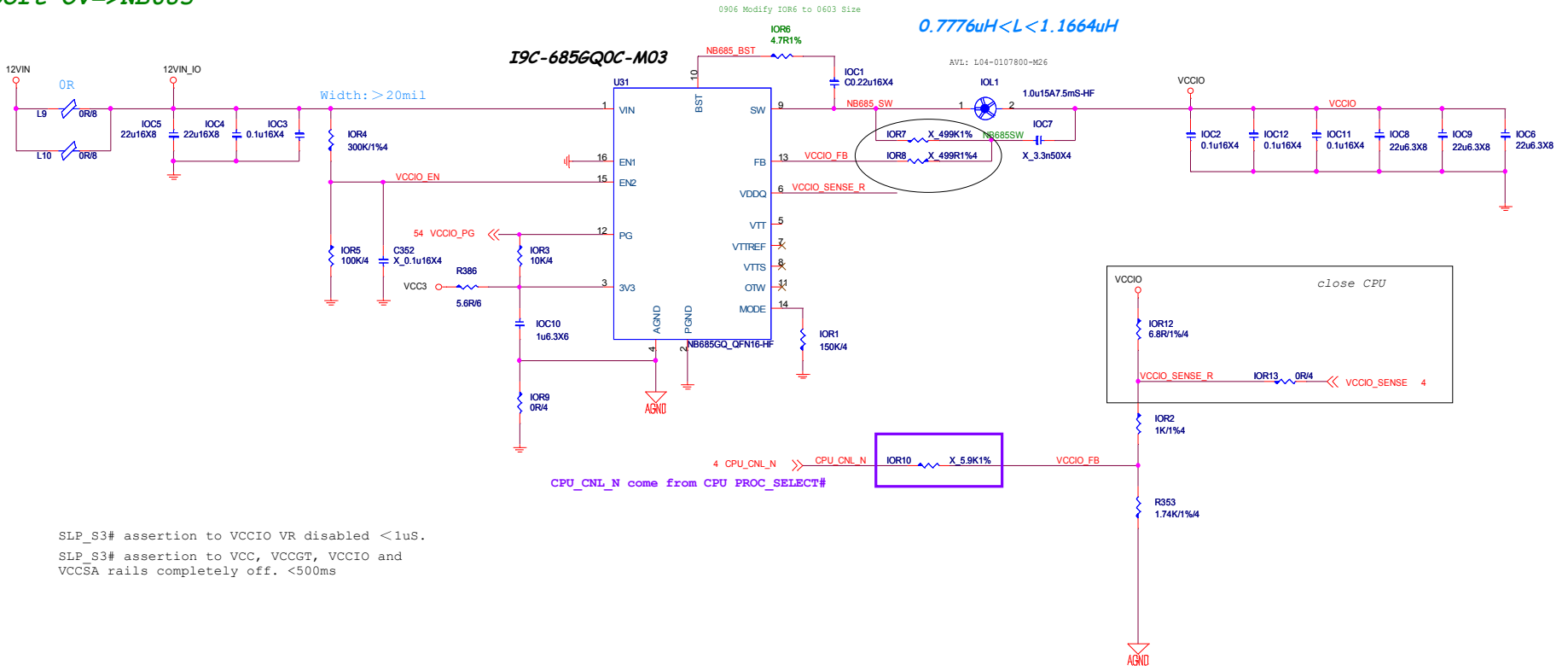
MICRO-STAR INT'L CO.,LTD	
MS-7A64..	
Size: Custom	Document Description: VGT MOS-PHASE 1~2
Rev: 10	
Date: Wednesday, September 21, 2016	Sheet 57 of 69

VCCIO

0.95V; 5.5A

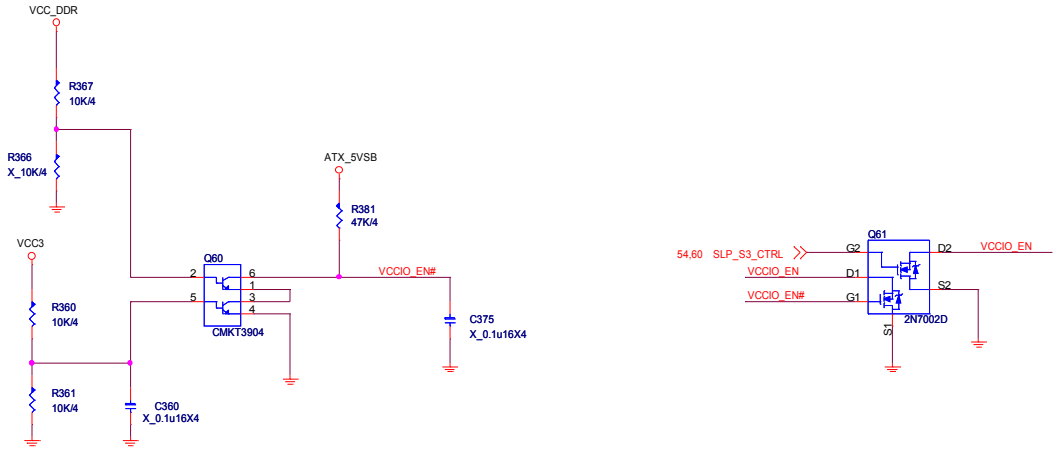
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

support OV=>NB685



SLP_S3# assertion to VCCIO VR disabled <1uS.

SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



SLP_S3# assertion to VR disabled max:1us

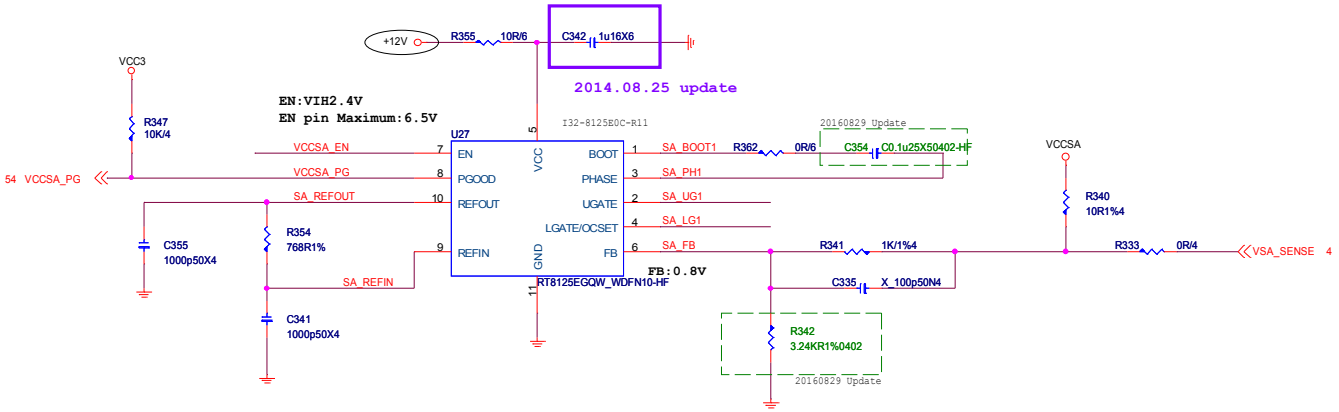
MICRO-STAR INT'L CO.,LTD		
MS-7A64..		
Size: Custom	Document Description: CPU PWR_VCCIO	Rev: 10
Date: Wednesday, September 21, 2016	Sheet 58 of 69	

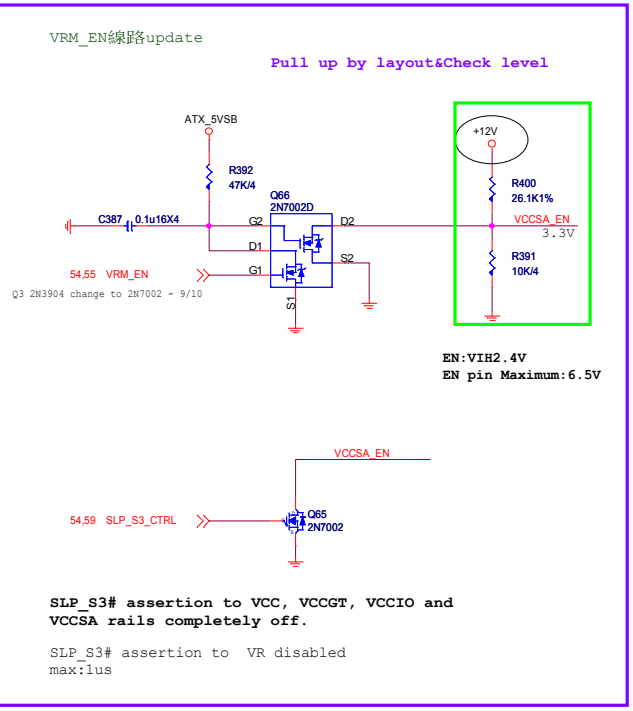
SA Power:1.05V,11.1A

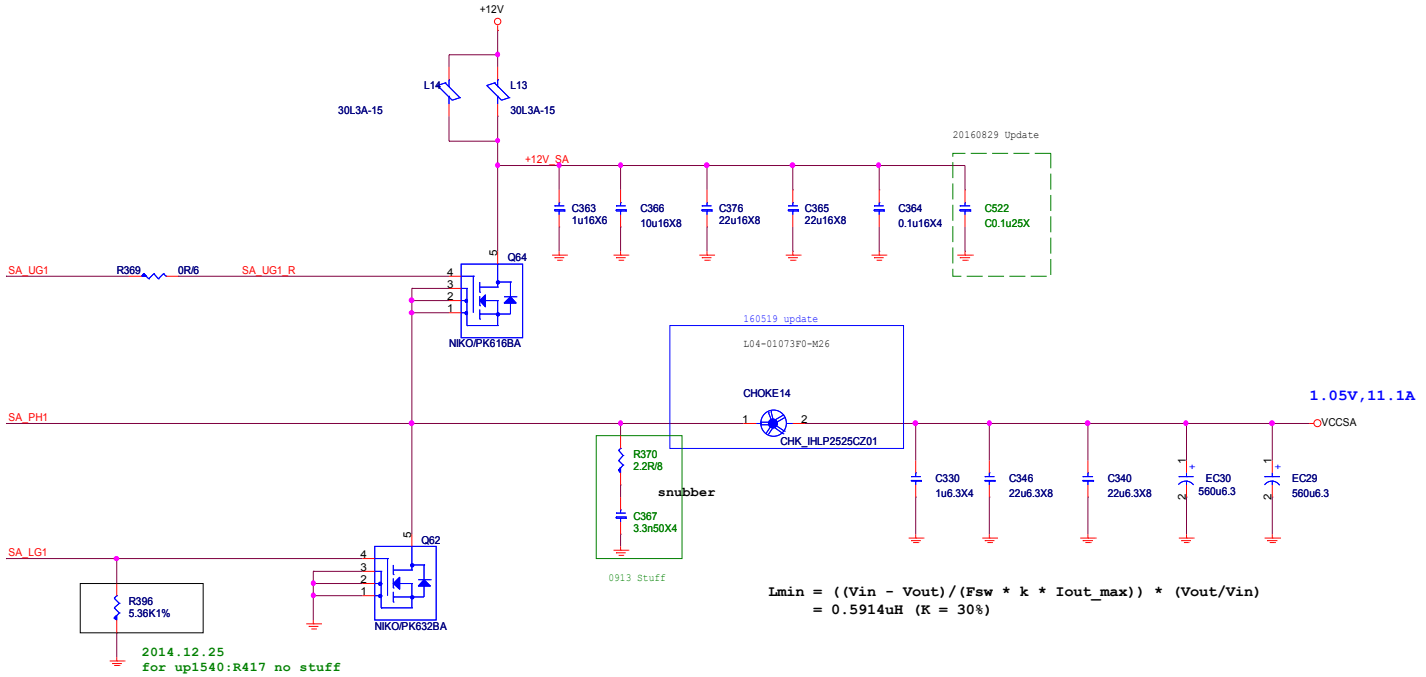
*OCP =11.1A*1.4=15.54A*
*Rocs(R417)=OCP*Rdson(Low side)3.4mohm]/10uA*
=15.54(3.4)mohm/10uA*
=5.2836Kohm

Rocs:5.2836K,OCP:
D03-4C05N03-O05 : 15.76A
D03-632BA0C-N03 : 16.24A
use UBIQ MOS need Check

Rdson(low)10V
D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm







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MS-7A64..

Size	Document Description	Rev
Custom	CPU PWR_SA-RT8125C	10

Date: Tuesday, September 20, 2016 Sheet 59 of 69

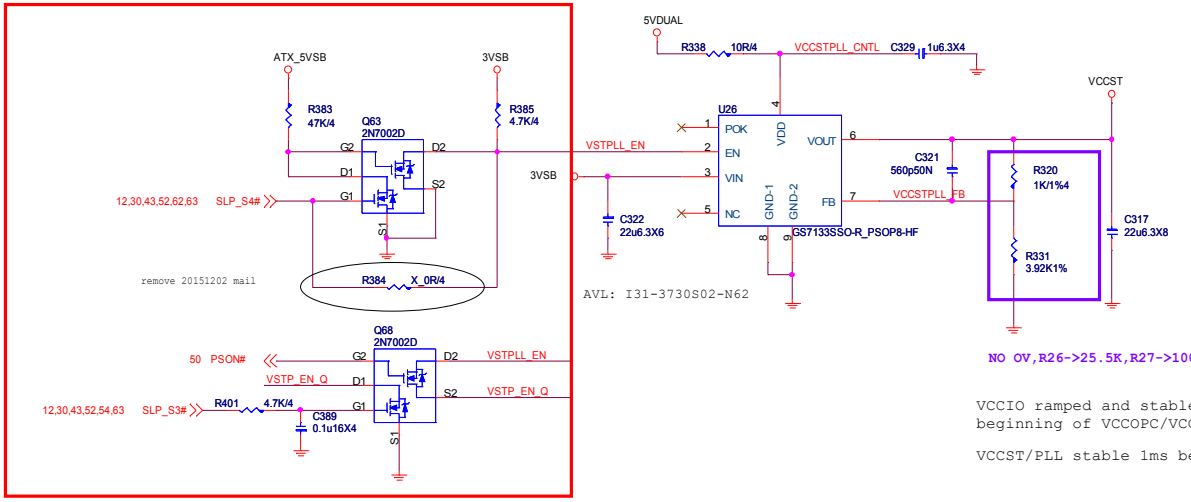
VCCST

for Gaming3/5, Classic, ECO and H110

VCCST:60mA
VCCPLL:150mA

1.0V; 210mA

For Cost down VCCST&VCCPLL merge



NO OV,R26->25.5K,R27->100K, C178 unstuff

VCCIO ramped and stable before beginning of VCCOPC/VCCEOPIO ramp

VCCST/PLL stable 1ms before PROCPWRGD

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	MS-7A64..	
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DDR4_1.2V 2.5A+9.5A+1.2A=13.5A

2.8A FOR CPU

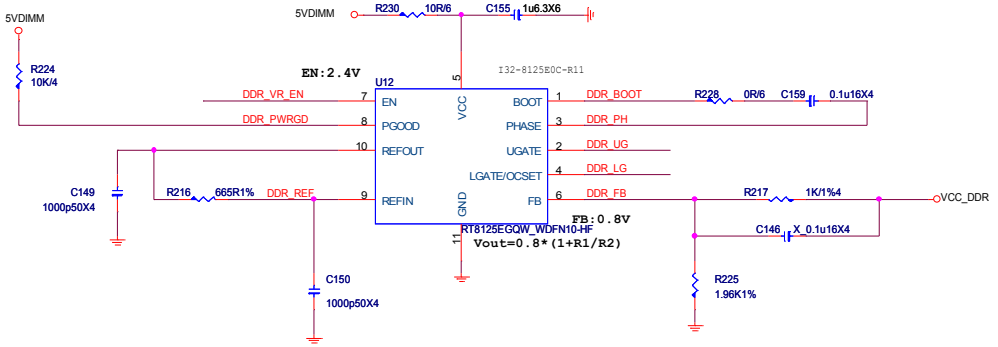
9.5A FOR 4DIMM

1.2A FOR DDR VTT

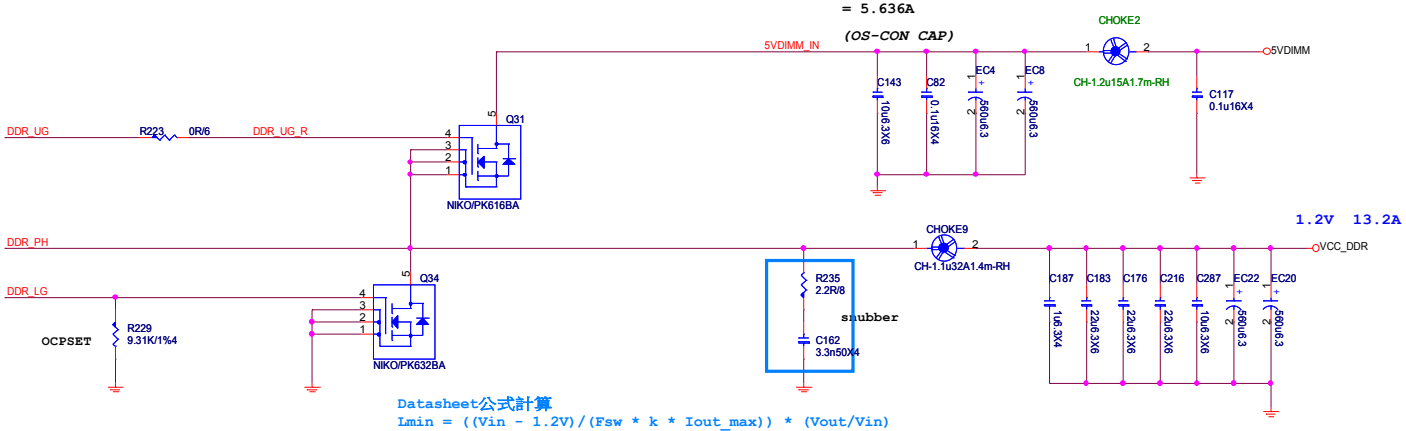
OCP =13.2A*1.5=20.25A
Rocs(R95)=OCP*Rdson[(Low side)]/10uA
=20.25A*(4.6)mohm/10uA
=9.315Kohm

Rocpset:5.1K
OCP=Rocset*Rdson[(Low side)]/10uA
=9.31K*(4.6)mohm/10uA
=20.23A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-4C05N03-005 : 5 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm



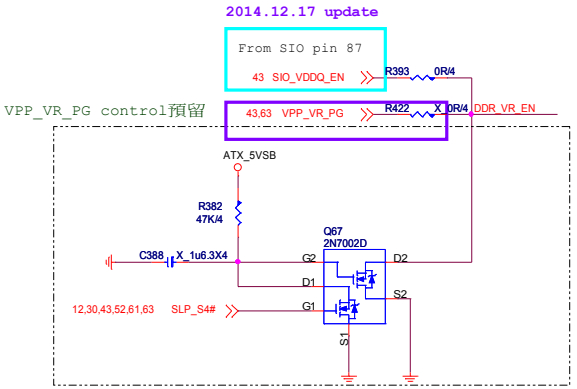
Irms = Iout * SQRT{(Vout/Vin) * [1 - (Vout/Vin)]}
= 13.2* 0.427
= 5.636A



Datasheet公式計算
Lmin = ((Vin - 1.2V)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.7677uH (K = 30%)

若帶入CAP ESR計算,0.2432uH＜L＜1.2897uH

2014.12.17 update



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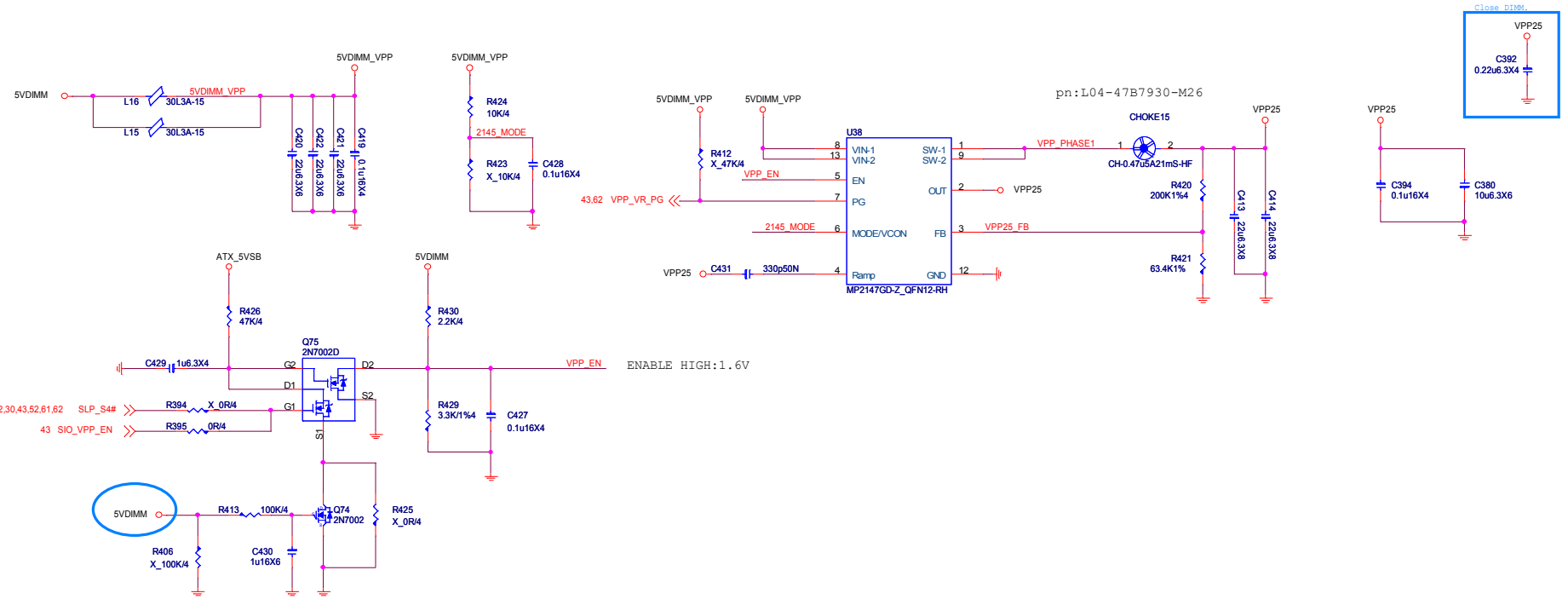
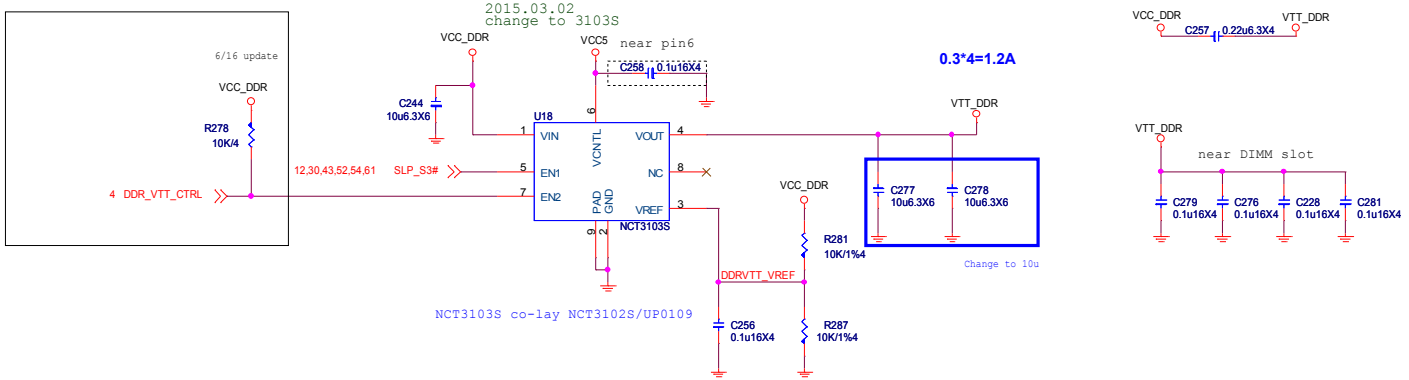
4DIMM :2.24A FOR DDR VPP2.5V

VPP25 Power

2.5V; 2.24A



DDR VTT Power



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PCH 1VSB

1.0V; 11.83A

OCP = 17.745A

Rocset = 1.5 * Imax * Rdson(low) / Iocset
= 1.5 * 11.83 * 4.6mohm / 10uA
= 8.16K

Rocs:7.87K,OCP:
D03-4C05N03-005 : 15.74A
D03-632BA0C-N03 : 17.1A
use UBIQ MOS need Check

Rdson(low)4.5V
D03-3116M00-U47 : 3.6 mohm
D03-632BA0C-N03 : 4.6mohm
D03-3056M00-U47 : 6.2mohm

1504 change to 8125 I32-8125E0C-R11

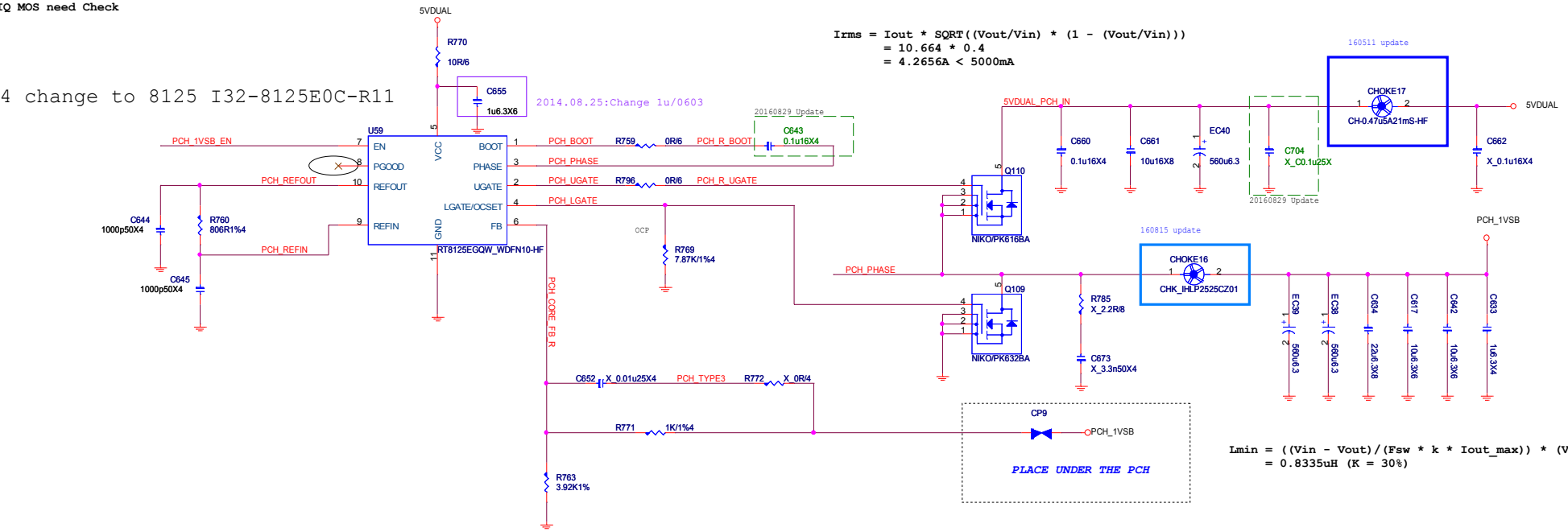
2014.08.25:Change 1u/0603

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 10.664 * 0.4
= 4.2656A < 5000mA

160511 update

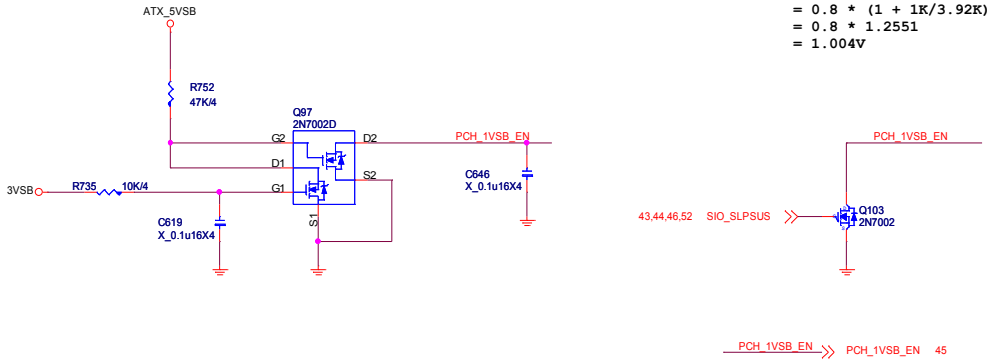
160815 update

20160829 Update



Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
= 0.8335uH (K = 30%)

Vout = Vref * (1 + R821/R822)
= 0.8 * (1 + 1K/3.92K)
= 0.8 * 1.2551
= 1.004V



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PCB

PCB1

7A64_0A

PD0-07A6410-G37

PD0-07A6410-E48

MK_LABLE1 — MARKET LABLE — MK_LABLE1

AMI_LABLE — AMI_BIOS LABLE — BIOS_LABLE

HDMI_LABLE — HDMI LABLE — HDMI LABEL

CFOS_LABLE — CFOS LABLE — CFOS_LABLE

NAHIMIC_LABLE — NAHIMIC LABLE — NAHIMIC_LABLE

SSE_LABLE — SSE LABLE — SSE_LABLE

USB31 — USB3.1 LABLE — USB31_LABLE

XSPLIT_LABEL — XSPLIT LABLE — XSPLIT_LABEL

Audio Small Cover

COVER1 — Audio Cover — E21-7978010-RH

CPU_H1 — CPU 鐵座 — CPU_H1

BAT1_X1 — BAT-BCR2032P-RH

Mounting Holes

MH1, MH2, MH3, MH4, MH5, MH6, MH7, MH8, MH9 — X_MH001

C691 0.1u16X4

C714 0.1u16X4

HS_MOS1 — MEC1, MEC2 — HS-0503710-RH

HS_MOS2 — MEC1, MEC2 — HS-0503720-RH

0912 Modify footprint same as E31-0408530-K08

PCH_HS — MEC1, MEC2 — msi — HS-0408530-RH

DDR_COVER1 — DDR COVER — X1, X2, X3, X4, X5 — E21-7A63010-RH

0906 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

VR_COVER1 — VR Cover — X1, X2 — E21-7A63020-RH

0919 Modify OE2-7A63001-A91 to E21-7A63020-A91

Simulation

VCC5 — SIM1 — X_PIN1*2 — SIM2 — X_PIN1*2

Test point

VCORE — VCORE1

VGT — VGT1

VCC_DDR — VCC_DDR1

VCCSA — VCCSA1

VCCIO — VCCIO1

PCH_1VSB — PCH_1VSB1

VCCST — VCCST1

VTT_DDR — VTT_DDR1

VPP25 — VPP1

Option BOM

Page 12~17 — OPCH1 — PCH — X_B250

MKLABLE2 — MARKET LABLE — X_MKLABLE_B250

Page 33,36 — OUH1 — HDMI — X_HDMI

M2_2 鐵片 — M2_H1 — M2 鐵片 — M2_H1 — 0919 Add

M2_2 SCREW — SCREW2 — SCREW — SCREW

M2_1 SCREW — SCREW1 — SCREW — SCREW

Optical Fiducial Marks-120

FM1, FM2, FM3, FM4, FM5, FM6, FM7, FM8 — X_FM

EMI CAP

VCC3 — C781 X_0.1u16X4

VCC5 — C772 X_0.1u16X4

VCC5 — C773 X_0.1u16X4

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